Post-CMOS Micromachining of Surface and Bulk Structures

Xu Zhu

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To My Parents

and To My Wife, Wei.

“All models are wrong; the practical question is how wrong do they have to be not be useful.”

George E. P. Box and Norman R. Draper

Empirical Model-Building and Response Rurfaces

Abstract

This thesis describes fabrication of the micro-electro-mechanical system (MEMS) through post Complementary-Metal-Oxide-Semiconductor (CMOS) micromachining. It focuses on device fabrication instead of device designs. The reactive-ion-etch (RIE) and deep-reactive-ion-etch (DRIE) are key technologies in this process flow. Surface micromachining of the thin-film dielectric material and bulk micromachining of the Si substrate are discussed in detail. Fundamentals of the RIE and DRIE dry etch, the methodology to characterize these process techniques and the design of experiments (DOE) to discover processing windows for post-CMOS micromachining are illustrated. Experimental results of the processing characterization are translated to MEMS design rules. These rules serve as a protocol to qualify the process as a common platform and to verify MEMS device designs to be build on this platform. Migrations of post-CMOS micromachining have been demonstrated with advances of CMOS fabrication: from a 0.5 μm process to a 0.18 μm process, from an aluminum (Al) interconnect silicon-dioxide (SiO_2) dielectric process to a copper (Cu) interconnect low-K dielectric process. Different CMOS foundry services in the United States, Europe, and Asia, have been selected to successfully fabricate MEMS devices. Starting with small chips at the size of 2 mm × 2 mm, post-CMOS micromachining can be performed at the wafer scale with an add-on low resolution photoresist mask layer. An integrated dicing scheme into the post-CMOS process flow has been documented. A wet chemical cleaning step can be inserted into the process flow to remove etch by-products in RIE therefore improves the quality of the process. The application in areas of the high-performance inertial sensor and high-quality passive radio-frequency (RF) components are demonstrated.

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1

Introduction

The Micro-Electro-Mechanical System, known as MEMS in the US, is becoming a methodology for building a complicated system which integrates physical, chemical, bio-medical and electronic components on a single chip. It merges the functions of computing and communication together with sense, actuation and control, and completely changes the way people and machines interacting with the physical world [1]. Miniaturization is the key feature for all MEMS devices compared to their macro-world counterparts. It enables a very-large-scale integration (VLSI) of devices with different functionalities into one package: a high-functionality system which can achieve higher-level performance, complexity and versatility than its embedded individual components. The direct impact of VLSI allows that systems to be batch fabricated, leading to low-cost for each unit. Moreover, these systems consume low-power and are light weight versus their macro-scale counterparts. Reliability and robustness can be much better improved due to the inherent advantage of miniaturization and by large volume fabrication. Furthermore, these highly-functional MEMS systems can be easily embedded into higher level systems so that more complicated tasks can be completed. The growth of MEMS not only borrows many concepts, techniques and processing equipment from the semiconductor industry, but also is following the same path as the semiconductor industry which grew from building single discrete transistors to building highly integrated information networks.

MEMS covers a wide range of research areas and commercial applications [2][3], which include sense, actuation, materials and material properties, process techniques and equipment, computer-aided-designs (CAD), packaging and system integrations. Because of the nature of MEMS, researchers involved in this area come from all areas of engineering and science. MEMS has grown from a scientist’s dream 40 years ago [4] to government funded research projects 10 years ago to being an intricate part of many commercial products today.

While most research efforts in MEMS focus on new concepts, new designs, new materials and new process technologies, attention has not been paid to the construction of manufacturing infrastructure. Only a few prestigious universities and companies have MEMS fabrication facilities. This situation is also due to the diversity of MEMS fabrication technologies, the low volume of manufacturing and the high cost of maintaining cleanrooms. As the MEMS research covers such a wide spectrum, and so many technologies have been developed, most of them still in embryonic stages, most MEMS devices cannot be high-volume batch fabricated. Some companies have successfully commercialized MEMS technologies, such as the polysilicon surface micromachined inertial sensors adopted by Analog Devices Inc.. However, due to limited fabrication capabilities and a highly competitive market, these commercial companies offer outside users only limited access to their production lines. There are some small MEMS foundry services in the market, *e.g.*

the MUMPS® [5] process service from Cronos Integrated Microsystems Inc., but low-volume fabrication and acquisitions make it difficult for them to remain independent as foundries. Another difficulty, which small companies have to face soon, is the size of the wafer handled by equipment. Currently, the mainstream wafer size in the semiconductor industry is 8-inch, and it is migrating to the 12-inch level [6]. But top-end MEMS production lines are still at the 6-inch level. This is because that low-volume production does not require and can not afford upgrading to new processing tools. Although some universities consolidate together to offer foundry services, because the purpose of these facilities is for the academic research, they cannot be converted into commercial services. Furthermore, complicated fabrication details and different requirements in different universities induce a slow learning curve. Even some organizations, *e.g.* MEMS Exchange℠ [7], act as "trusted intermediary" between the fabrication service providers and the user community, and offer MEMS help or expertise, a lot of detailed processing issues still cause the significant consumption of end-user design efforts.

Many end users, both in industry and academic, now consider developing a MEMS solution or incorporating one into a system design. Usually, they want to explore possibilities of new functions, significant reduction in cost, or both which can be obtained through the MEMS technologies, not to develop a new MEMS technology or demonstrate a new concept as in initial stages of MEMS. They prefer evaluating basic concepts of a new product through existing designs and foundry services, not building everything from scratch. Moreover, more and more traditional semiconductor companies are spinning off their fabrication facilities, outsourcing the production manufacturing and converting into design houses to reduce the operation cost. For example, Advanced Micro Devices, Inc. (AMD), the No. 2 company in microprocessor design and fabrication, will outsource 25% of their production [8]. This business model definitely affects the decision on the construction of MEMS infrastructures. Obviously, a public accessible infrastructure not only helps the growth of MEMS itself, but also expedites the acceptance of MEMS solutions in real world applications.

Currently, many researchers have demonstrated that different MEMS devices can be fabricated based on or through Complementary Metal-Oxide-Semiconductor (CMOS) fabrication processes with add-on post CMOS steps. Because there are few equipment requirements for post CMOS micromachining and it does not disturb normal CMOS processes, numerous semiconductor manufacturing facilities can be used as a MEMS fabrication platform.

Leveraging on CMOS foundry processes, MEMS structures, which are built by microelectronic fabrication, have multiple CMOS dielectric layers (silicon dioxide in most cases), polysilicon layers, and interconnect metals (aluminum in most cases). As a common practice, MEMS users submit their designs to a multiple-user CMOS fabrication project, *e.g.* MOSIS® service, and receive their chips back several months later. Rather than whole wafers, the samples are usually 10 to 50 units of several square millimeters of silicon. Generally, it is very difficult to do photolithography on these chips, due to the challenge of uniformly coating the chips with photoresist and patterning fine structures. There are several approaches to solve these problems:

- The first one is to use a backside etch [9][10][11][12][13]. This includes depositing mask materials on the back of the chips, followed by a low resolution photo lithography. The etching is conducted from the back. Either a wet etch [*e.g.* potassium hydroxide (KOH), ethylenediamine-pyrocatechol (EDP) or tetramethyl ammonium hydroxide (TMAH) solutions] or a dry etch [*e.g.* Xenon difluoride (XeF_2)] can be applied to etch silicon (Si). The etch is stopped either by etch resist layers (*e.g.* heavily doped silicon or dielectric) or by a time controlled etch, and results in membrane structures.
- Another approach is to expose the polysilicon layers and undercut the oxide beneath the polysilicon [14][15][16]. The resulting polysilicon structures are similar to those produced by polysilicon surface micromachining. However, the residual stress induced buckling in polysilicon layers is a challenge because the polysilicon layer in conventional CMOS is less than 1 μm above the Si substrate and the residual stress in polysilicon is beyond the user's control.
- The third approach is proposed by research groups in both Europe and North America [14][17]. Si is the sacrificial material in this process. The stacking of active areas, metal contact cuts and cover glass cuts leaves bare silicon ready for post-CMOS processing. Again, KOH, EDP and TMAH, and XeF_2 can be used to etch the Si substrate. Similar approaches used on Gallium Arsenide (GaAs) substrate processes have been reported as well [18]. Example applications include thermal type devices (*e.g.* infrared sensors [19][20][21], electrothermal converters [22][23], and voltage regulators [24]), piezoresistive gauges [25][26] (*e.g.* accelerometers, tactile sensors, pressure sensors, magnetic

sensors), passive RF components (*e.g.* on-chip inductors [27][28]), optical system components [29] and *in situ* processing characterization [30]. All the mechanical structures mentioned in the above examples fall into two categories: a fixed-fixed beam structure or a cantilever structure. Furthermore, this approach cannot be implemented on the chips fabricated in a Damascene process, which adopts chemical mechanical polishing (CMP) to define interconnects.

- The fourth approach in post-CMOS micromachining is being developed at Carnegie Mellon University, and it will be discussed in detail in the rest of this thesis. Different from the third method, MEMS structural layouts in this last option are fully compatible with CMOS design rules. In order to expose the silicon substrate, top metal layers are used as etch-resist masks to delineate mechanical structures and prevent the circuitry from being etched out during post-CMOS microfabrication [31][32][33][34]. Figure 1-1 describes the basic process flow. A three-metal one-polysilicon CMOS process with CMP is assumed in Figure 1-1. Unlike other aforementioned approaches, this fabrication flow requires only reactive ion etch (RIE) dry etch processes, which are widely used in CMOS fabrication. Beginning with the dice from a CMOS fabrication service, Figure 1-1(a), the etch starts with a CHF_3/O_2 anisotropic RIE etch of dielectric layers, resulting in Figure 1-1(b). The entire process flow is completed by a time-controlled SF_6/O_2 isotropic etch of the underneath silicon to release the mechanical structures, as in Figure 1-1(c). The mechanical structures are outlined by the top CMOS interconnect metal layers. The multi-layer structures consist of one or two polysilicon layers, three or

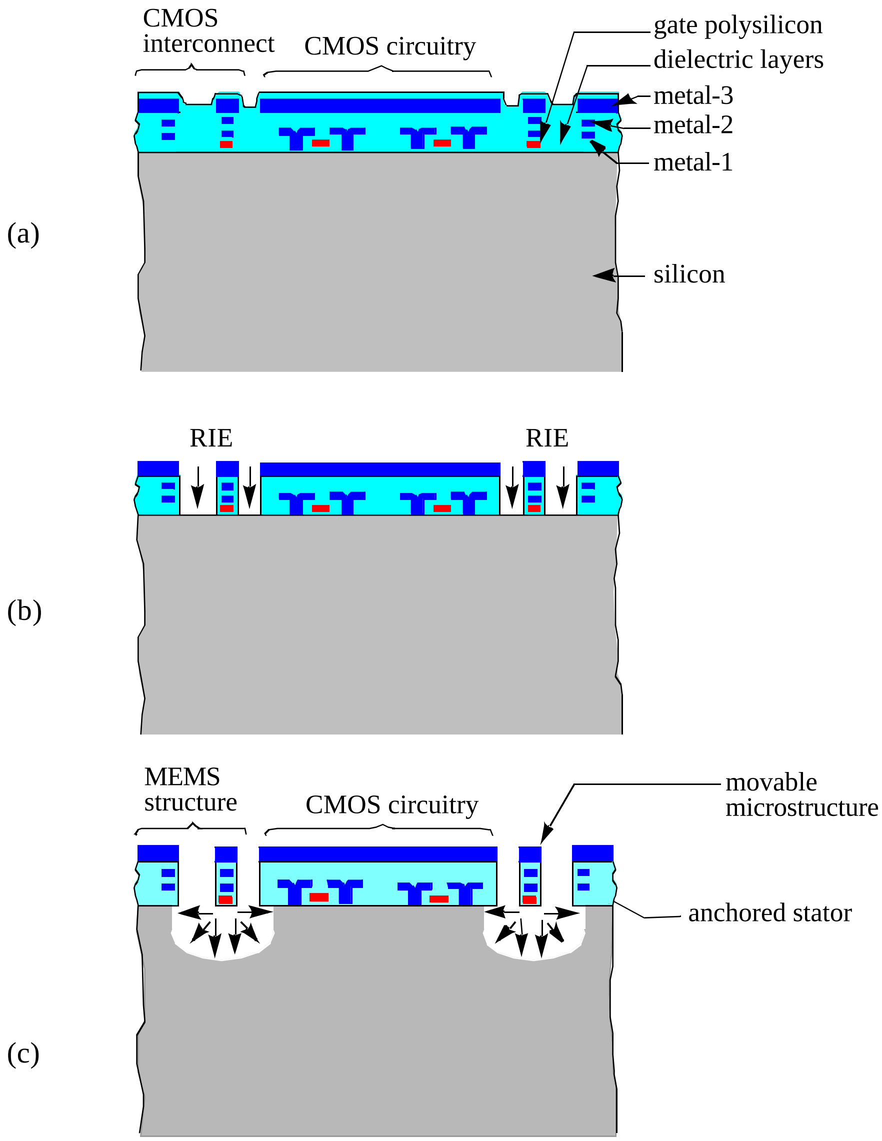

CMOS interconnect
CMOS circuitry
gate polysilicon
dielectric layers
metal-3
metal-2
metal-1
silicon
(a)
RIE
RIE
(b)
MEMS structure
CMOS circuitry
movable microstructure
anchored stator
(c)

Figure. 1-1. **Cross sections of device in each stage of the process flow.**
(a) Device from CMOS processing.
(b) Anisotropic dielectric layers etch.
(c) Isotropic Si substrate etch to complete the process flow, resulting integrated MEMS structures with CMOS circuitry.

even more metal layers and the inter-metal dielectric layers. This process requires no photolithography, and it is a self-aligned process. Obviously, the mechanical structures can be defined very accurately, below one micron by modern CMOS

> fabrication lithography. Compared with wet etching, this process does not require any rinsing and drying steps. Another of its unique features is that its thin-film structures, a characteristic of surface micromachining devices, are formed by the bulk micromachining steps. “Stiction” problems, which exist in surface micromachining, are not present in this last option [35]. However, there is a drawback in these multi-layer structures: the CMOS composite films have stress-gradient induced curling. This problem can be alleviated by design efforts. Overall, like the other approaches, without changing or inserting process steps into CMOS fabrication sequences, this technique enjoys the capability to use enormous commercial microelectronic fabrication services as a MEMS manufacturing platform, and it can be appended to any new fabrication technology. As a result, this approach will lead to more MEMS applications, and reduce both the time and the cost for MEMS prototyping.

This thesis focuses on integration issues of the last post-CMOS MEMS fabrication process option described in previous paragraphs. Beginning with a small size chip, around 2 mm × 2 mm, and an aluminum (Al) interconnect silicon-dioxide (SiO_2) dielectric, challenges are then extended to a whole wafer process and a copper (Cu) interconnect low-K dielectric. Included in the following chapters are the technical details of this process, the methodology to solve process and integration difficulties, a demonstration of experimental results, and MEMS design rules to serve end users who are designing MEMS in CMOS.

Other approaches [36][37][38][39][40][41][42][43][44] require depositing extra materials and modifying CMOS fabrication. These are out of the scope of this thesis and will not be discussed in the following chapters.

Two terminologies are clarified here: surface micromachining and bulk micromachining. Following conventions in the literature [45], the microfabrication into the thin-film above the substrate is called surface micromachining; and the microfabrication into the substrate is called bulk micromachining. By this convention, the dielectric layer etch is surface micromachining, and Si substrate etch, isotropically or anisotropically, is bulk micromachining. Obviously, the process flow shown in Figure 1-1 is a combination of surface micromachining and bulk micromachining, and it results in a thin film structure with the characteristic of surface micromachining devices. However, some modifications in this process flow yields final MEMS devices with the bulk Si materials, as shown in the later chapters.

Chapter 2 focuses on RIE micromachining of thin dielectric films. After the introduction of physical and chemical processes in RIE, a parallel-plate RIE system is briefly described. The major difficulty of RIE of SiO_2 in the post-CMOS MEMS process is the multiple stringent requirements. A design-of-experiment (DOE) methodology is used to solve this problem. The mathematical model, precisely predicting the process direction, is developed with this methodology, and is verified by measurement data. RIE etch lag problems are explored with current MEMS structures, which lead to processing considerations.

Chapter 3 describes bulk Si micromachining, including both isotropic and anisotropic Si etch. Instead of using a parallel-plate RIE system as in the original publication [31], a new processing tool, inductively coupled plasma (ICP), is introduced to speed up the process and to obtain higher yields for the process. The basic concept of ICP system is described first. Then the Bosch deep RIE (DRIE) high-aspect-ratio Si etch technique, which is used to achieve anisotropic etch in the process, is described. The characterization of DRIE etch lag is highlighted. The Si isotropic etch using the ICP system is the most critical step in the process because it determines the final released structures. Therefore, the entire process space of the etch is explored by DOE and the etch behavior is thoroughly characterized.

Chapter 4 first discusses the necessity and importance of MEMS design rules. Then by analyzing the typical device layout, three commonly used geometric patterns are identified and three test structures designs are proposed. The method of effectively collecting data on these structures are illustrated. A set of design rules is therefore derived at the end of this chapter.

Chapter 5 discusses the detailed practical issues related with this post-CMOS micromachining. These include cleaning polymers deposited on the sidewall of microstructures and tuning this process to be suitable for a state-of-art Cu interconnect low-K dielectric material process. Issues of developing a wafer-scale process, compared with a single small sample, are also discussed in this chapter. The modified process flow with an embedded dicing scheme is presented here.

Chapter 6 gives two examples of post-CMOS micromachining. In the first example, different technologies are compared and performance improvements on on-chip inductors in the quality factor are highlighted. The finite-element-method (FEM) physical model and lumped circuit model are used to explain inductor behaviors. Performance enhancement limitations are predicted. The second example is a bulk accelerometer. Compared with thin film devices, a different design philosophy is emphasized. Demonstrated here is the significant reduction of residual stress induced curling. The device performance is briefly summarized.

In Chapter 7, the enhanced and characterized process flow is summarized. Different successfully fabricated MEMS devices through various CMOS foundry services are demonstrated. The future work to improve the post-CMOS microfabrication technology and to explore the new application of this technology is proposed.

2 Dielectric Thin Film Micromachining

2. 1 INTRODUCTION

Described in Figure 1-1, the dielectric layer etch is the first step in the post-CMOS micromachining process sequence, and it is currently implemented by RIE. This process flow yields composite mechanical structures made of layered thin film. As illustrated Figure 1-1, some of these materials, *e.g.* SiO_2, are also the materials being etched. Currently, there are several techniques for removing materials in CMOS fabrication processes: CMP, wet etch, ion milling and RIE.

- CMP is a process technique being developed together with the copper Damascene process [46][47][48]. It removes excess metal interconnect materials from the trench fill deposition in Damascene processes, and results in planarized metal lines engraved in dielectric films. The planarizing of the surface is required for deep sub-micron photolithography, in which the optical system focal length is extremely short and any surface topology is not allowed. CMP provides a global large removal and doesn’t suit the process requirements for defining released microstructures.

- Wet etch was once widely used in the semiconductor fabrication. In the MEMS industry, wet etch is used to etch sacrificial layers, *e.g.* silicon dioxide in polysilicon surface micromachining. It has a very fast etch rate and doesn’t require very sophisticated process equipment for batch fabrication. However, wet etch usually leads to an isotropic profile with most dielectric materials used in microelectronic fabrication, and fine features with a high aspect ratio cannot be obtained.
- Ion milling can achieve good directionality, but its physical bombardment nature determines its poor selectivity between the material being etched and the etch resist mask. The low etch rate is another draw back of this technology.
- RIE, sometimes called ion-assisted etch, combines characteristics of fast etch rates, high selectivities and accurate profile controls. These characters made RIE the most favorable etch fabrication technique in modern micro-fabrication processes, and is therefore our choice for post-CMOS micromachining.

In this chapter, physical and chemical mechanisms involved in RIE processes are first described. The critical processing parameters related to a parallel-plate RIE system configuration are illustrated. Challenges of RIE of dielectrics in the post-CMOS process are identified. A methodology to overcome these difficulties is discussed, and is demonstrated with experimental data. The major effects, which characterize the process, are discussed first, followed by second order parameters. At last, a main process concern, etch lag effect, is quantified, and the guideline to handle the etch lag effect in the structure layout and processing is given.

2. 2 MECHANISM OF RIE PROCESS

RIE is a widely used dry etch process technique in modern semiconductor processing. Its relation to other dry etch techniques, as it was defined in the late 1980s’, is illustrated in Figure 2-1. With the advance of fabrication equipment, the criterion to distinguish the three primary dry etch processes, physical etching, RIE and plasma etching, may not be as clear as indicated in the Figure 2-1. For example, in an Electron Cyclotron Resonance (ECR) tool or an Inductively Coupled Plasma (ICP) tool, the processing pressure of the RIE mode is usually in the 1 mTorr ~ 10 mTorr range, while the pressure of the plasma etch mode can go below 100 mTorr. However, in general, the definition in Figure 2-1 is still valid for most cases, and the parallel-plate RIE system used for the dielectric etch in this thesis work falls into this spectrum.

Figure 2-2 describes the basic physical and chemical mechanism in RIE. It has seven basic steps. Reactive species (ions, radicals, etc.) are generated in a plasma environment

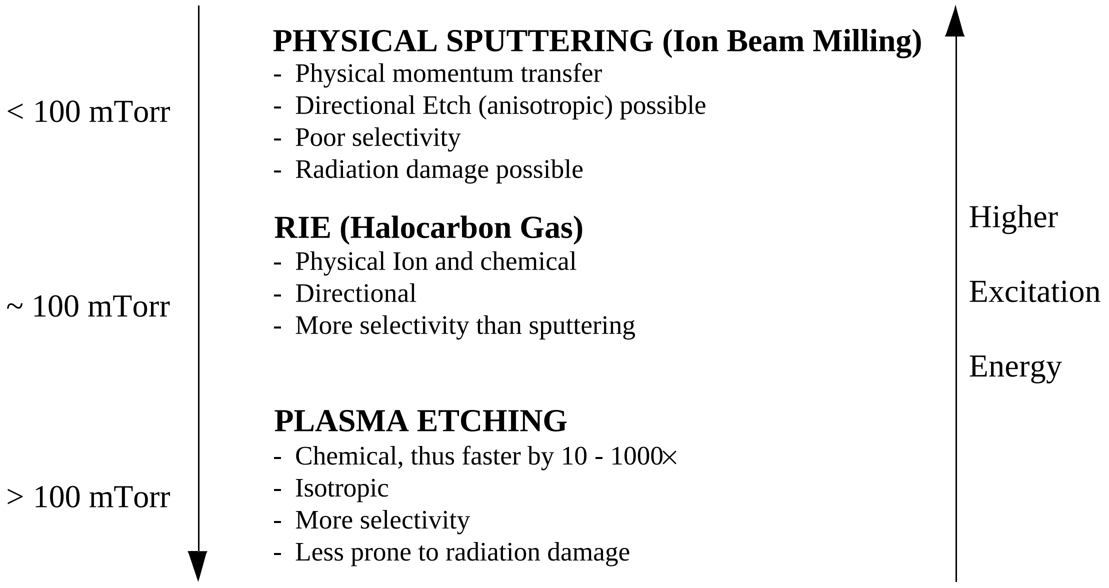

< 100 mTorr
~ 100 mTorr
> 100 mTorr
PHYSICAL SPUTTERING (Ion Beam Milling)
- Physical momentum transfer
- Directional Etch (anisotropic) possible
- Poor selectivity
- Radiation damage possible
RIE (Halocarbon Gas)
- Physical Ion and chemical
- Directional
- More selectivity than sputtering
PLASMA ETCHING
- Chemical, thus faster by 10 - 1000×
- Isotropic
- More selectivity
- Less prone to radiation damage
Higher
Excitation
Energy

Figure. 2-1. **The dry etching spectrum[49].**

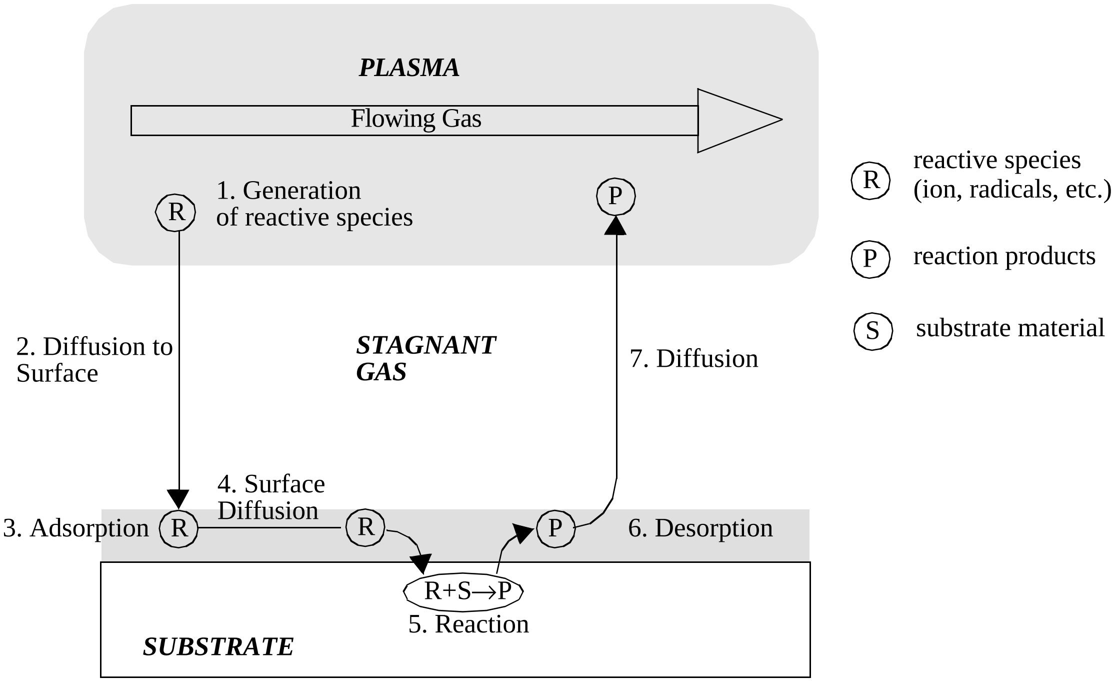

PLASMA
Flowing Gas
R
1. Generation
of reactive species
P
2. Diffusion to
Surface
STAGNANT
GAS
7. Diffusion
3. Adsorption
R
4. Surface
Diffusion
R
P
6. Desorption
R+S→P
5. Reaction
SUBSTRATE
R
reactive species
(ion, radicals, etc.)
P
reaction products
S
substrate material

Figure. 2-2. **Schematic representation of the seven basic steps in spontaneous plasma etching[50].**

by excitation, dissociation and ionization. These particles reach the substrate surface either by diffusion (radicals) or external electric field (ions). Radicals subsequently absorb on the surface, while molecular ions, with their momentum, may disintegrate upon impact and penetrate the surface slightly (ion mixing). Due to surface diffusion, the reactions may or may not happen on the sites where the particles land. A large variety of different reaction paths can occur. Finally, the reaction products will leave the surface, either by desorption if the by-products are volatile or by ion-activated processes, and diffuse back into the plasma [49][50][51].

Generally, there are two types of chemical processes: the homogeneous gas-phase collision and the heterogeneous plasma-surface interaction. The homogeneous gas-phase collision is responsible for the production of reactive free radicals, metastable species, and ions. The heterogeneous reaction occurs between these species and the solid substrate surfaces. Typical reactions are listed in Table 2-1 [49]. *(AB)* represents gas molecules, and *A* (or *B*) represents dissociated atoms of gas molecules in plasmas. *(AB)** and *A** are excited states of *(AB)* and *A*.

In general, a plasma can be loosely described as an assembly of positively and negatively charged particles that is electrically neutral on a macroscopic scale. However, there are large local fluctuations due to different polarities of particles. The composition and relative concentration of individual constituents are determined by process parameters, such as the pressure, the residence time in the reactor, the reactor geometry, the applied voltage, and the magnetic field. The positively charged particles are mostly in the form of singly ionized neutrals, (i.e., atoms, radicals, or molecules) from which a single electron has been removed. The majority of negatively charged particles are usually free electrons not electro-negative ions. However, radicals are much more abundant in a glow discharge than ions because they are generated at a higher rate, due to low threshold energy. Radicals also have longer lifetimes than ions. But the relative fluxes of these two classes of particles can be comparable, because ions move much faster than radicals as a result of the kinetic energy gained from applied electric field, while the radical flux towards the substrate is determined solely by diffusion. Radicals, even neutral in charge, have a greater tendency to chemisorb on surfaces than their parent molecules, because of their unfilled outer electron shell.

Table 2-1: **Homogenous and Heterogeneous Reactions Occurred in the Plasma**

Homogenous		Heterogeneous	
Excitation	$e^- + (AB) \Rightarrow (AB)^* + e^-$ $(AB)^* \Rightarrow (AB) + h\upsilon_F$ $e^- + A \Rightarrow A^* + e^-$ $A^* \Rightarrow A + h\upsilon_F$	Atom Recombination	$(S - A) + A \Rightarrow S + A_2$
Dissociation	$e^- + AB \Rightarrow A + B + e^-$	Metastable De-excitation	$S + M^* \Rightarrow S + M$
Ionization	$e^- + (AB) \Rightarrow (AB)^+ + 2e^-$	Atom Abstraction (etching)	$(S - B) + A \Rightarrow S^+ + (AB)$
Dissociative Ionization	$e^- + (AB) \Rightarrow A^+ + B + e^-$ $e^- + (AB) \Rightarrow A^+ + B + e^-$ $e^- + (AB) \Rightarrow A^+ + B^+ + 2e^-$	Sputtering (etching)	$(S - B) + M^+ \Rightarrow S^+ + B + M$
Dissociative & Attachment	$e^- + A_2 \Rightarrow A^+ + A^- + e^-$	-	-
Dissociative Recombination	$e^- + (AB)^+ \Rightarrow A + B$	-	-
Electron Attachment	$e^- + (AB) \Rightarrow (AB)^-$ $(AB)^- \Rightarrow A^- + B$	-	-

There are four basic etching mechanisms in plasma dry etch processes:

- *sputtering* - the ion energy mechanically ejects substrate materials;
- *chemical gasification* - thermalized radicals chemically combine with substrate materials forming volatile products.
- *Energetic ion-enhanced chemistry* - neutral radicals alone reaching the surface can not form a volatile product efficiently and energetic ions alter the substrate or product layer so that chemical reactions can gasify the material. Feature sidewalls receive minimal ion flux and reactions are directional (anisotropic) since the ion flux mainly bombards surfaces oriented parallel to the substrate.
- *inhibitor ion-enhanced chemistry* - an inhibitor film coats the surface forming a

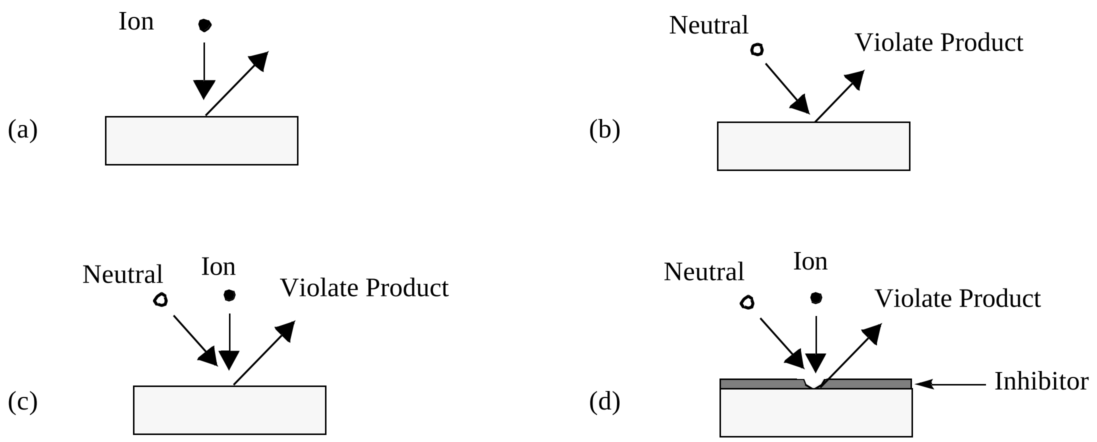


Figure. 2-3. **Four basic etching mechanism involved in RIE.**
(a) Sputtering.
(b) Chemical gasification.
(c) Energetic ion-enhanced chemistry.
(d) Inhibitor ion-enhanced chemistry.

protective barrier which excludes the neutral etchant. The moderate ion flux disrupts this protective film (on surfaces that are at right angles to the flux), allows chemical etching to proceed anisotropically, in the vertical direction, meanwhile the inhibitor film on the sidewalls protects them from attack [51].

However, these etching mechanism do not contribute equally in RIE processes. There are three major models for RIE: spontaneous etching [52], ion beam enhanced etching [53], and chemically enhanced physical etching [54]. In this paper, the first two model are used to explain the experimental results. In the first theory, the spontaneous etching is achieved by reactive neutral species, ion bombardment induced physical sputtering, or a combination. In the ion-beam enhanced etching theory, relative high energy impinging ions produce lattice damage at the surface being etched, create defects such as interstitials and vacancies, and at the same time, induce the mixing of the reactive radicals into the surface being etched. Moreover, the energetic particles' bombardment provide enough energy to desorb nonvolatile layers formed from reaction by-products (also referred to as surface inhibiting, or blocking layers) that deposit on the surface being etched. Despite the different explanations on the effects of ion bombardment, both theories assure that neutrals are responsible for almost all reactive etching, and that ions are rarely the etchant. In conclusion, RIE is an ion-assisted etching process.

2. 3 CONFIGURATION OF RIE SYSTEM

A typical Radio-Frequency (RF) powered RIE system is shown in Figure 2-4. It consists of two electrodes enclosed in a vacuum system. The bottom electrode is connected to a RF power source and isolated from the rest of the system. The top electrode is connected

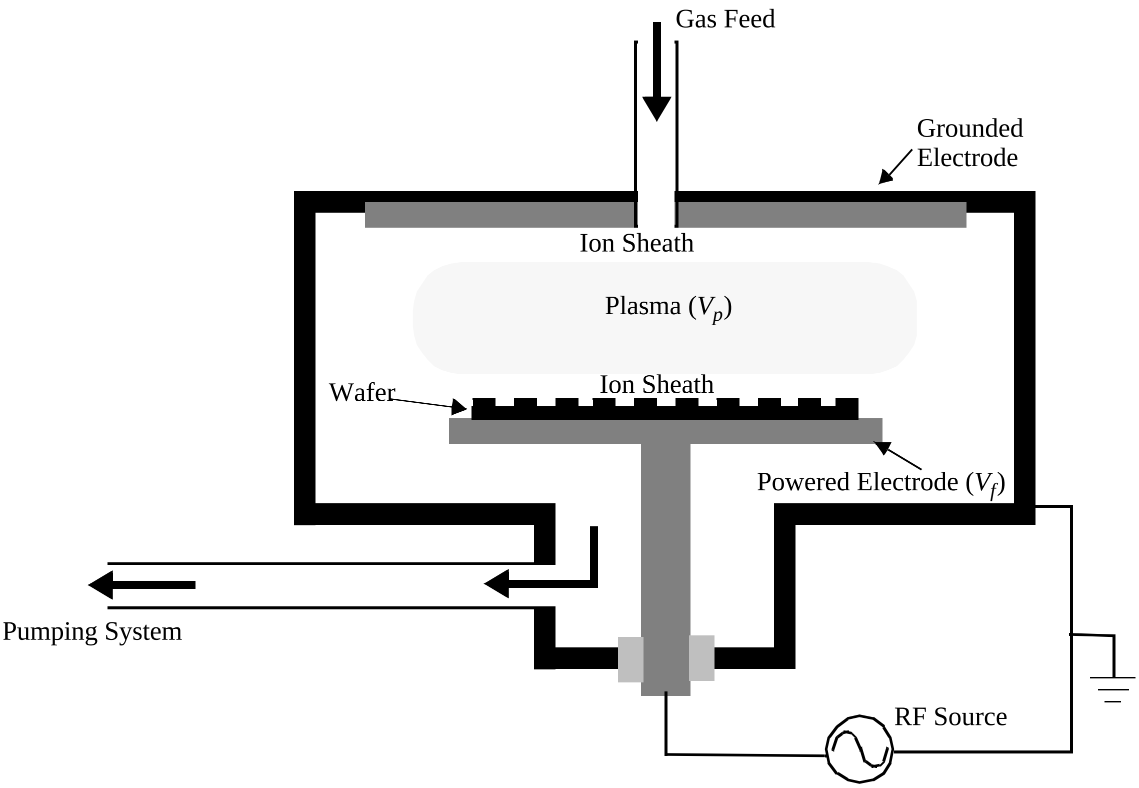

Gas Feed
Grounded Electrode
Ion Sheath
Plasma (V_p)
Wafer
Ion Sheath
Powered Electrode (V_f)
Pumping System
RF Source

Figure. 2-4. **A diagram of RF-powered RIE system.**

the chamber wall and is grounded. The system has a provision for continuously introducing a feed gas, and a port for pumping. The RF source connected to the bottom electrode creates a plasma. All reactive species are generated in the plasma. Because electrons are lighter than ions, they diffuse faster. Moreover, they can obtain higher velocity from the electric field, therefore they can travel a much longer distance during the alternating of the electric field polarities. At contact regions of plasma, such as the grounded chamber wall or the electrode, electrons deplete and recombine much faster than the ions. The electron density is extremely low in these regions, resulting in low levels of excitation of the gas molecules in these areas, and forming a thin dark region, called the “sheath”. The potential of the plasma is positive to that of the grounded electrode and powered electrode as in Figure 2-5. In summary, the plasma is a region of uniform electrical potential, and virtu-

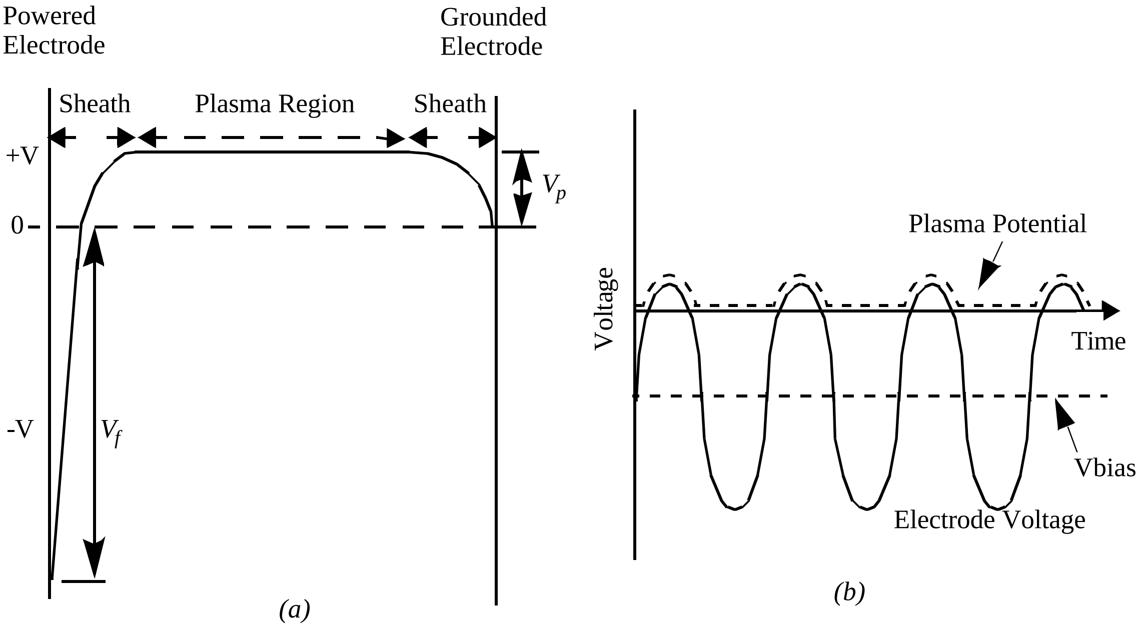


Figure. 2-5. Potential distribution in a parallel-plate plasma etcher with a grounded surface area larger than the powered electrode area.
(a) Potential distribution in a parallel-plate plasma etcher with a grounded surface area larger than the powered electrode.
(b) Potential on the RF-powered electrode and the plasma as a function of time.

ally all of the voltage change from the plasma to a surface or electrode occurs in sheaths, which are thin regions of high electric fields as well as current flow through the electrode surfaces. The magnitude of the self-bias voltage generated on the electrode is approximate half the applied peak-to-peak voltage. In the system with asymmetric areas of the ground electrode and the RF-powered electrode, a larger ratio of grounded electrode to the RF powered electrode yields a smaller potential difference between the plasma and the grounded electrode. Thus, the grounded surfaces are subjected to less energetic bombardment and less electrode material removal, resulting in less contamination of the wafer being processed. On the other hand, the wafer sitting on powered electrode is processed with higher energy bombardment and high efficiency.

For this type of RIE system, the operation pressure is between 1 mTorr to 2 Torr, the gas density ranges from 2.7×10^{14} to 2×10^{17} molecules/cm^3, the density of charged particles in glow discharge ranges from 10^9 to $10^{11}/cm^3$, and the fraction of ions-to-neutral species is thus about 10^{-4} to 10^{-6}. The average energies of electrons in glow discharges is between 1 to 10 eV.

2. 4 SILICON DIOXIDE ETCHING MECHANISM

Research on etching of SiO_2 was initiated when the mechanisms of plasma etching were being first studied. These studies conclude with two models to explain the chemical and physical mechanisms of RIE of SiO_2. These models are the fluorine-to-carbon ratio model [52] and the etchant-unsaturate model [53]. Details of these models are described in literature. In this section, they are utilized to understand the process and provide the knowledge for optimizing the process.

Generally, SiO_2 is etched by fluorocarbon gas, *e.g.* CF_4 or CHF_3. It is believed that both F atoms and CF_x radicals etch SiO_2. The F atoms spontaneously etch SiO_2, but the unsaturate-forming, “fluorine-deficient” CF_x radicals do not spontaneously etch SiO_2. Instead, it appears that F atoms are transferred to the substrate from a thin (≤ 10 Å) polymer layer that is formed when unsaturated fluorocarbon species impinge on the oxide surface, as in Figure 2-6. However, without ion-assisted, this polymer layer becomes so thick that no F atoms can penetrate through this layer to reach SiO_2 surface and conduct the reaction. The ions assist etch contributes in two factors:

- High energy ion impingement induces lattice damage, extending several monolayers beneath the surface. Ion damage produces dangling bonds and radical groups at the SiO_2 interface, where Si bonds are eventually converted into SiF_x groups. Exposed defects are covered with new polymers to accept active F based

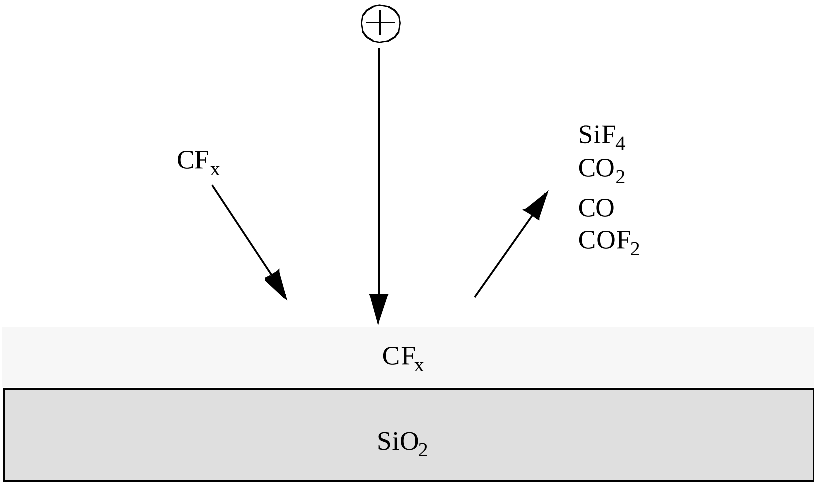


Figure. 2-6. During anisotropic etching of SiO_2, unsaturated radicals/species form a thin polymer layer on the surface, and halogen atoms are transferred to the substrate from this fluorocarbon layer.

radicals, resulting in further etching of SiO_2.

- Ion bombardment provides enough energy to desorb nonvolatile polymer layers on the surfaces being etched. In a process where polymer deposition occurs, surfaces not struck by ions do not have the blocking layer removed, and hence are protected against etching by the reactive gases. As described in Figure 2-4, ions come out from the sheath strike the wafer surface perpendicularly. Therefore, these ions remove polymer deposited on the bottom of etched features. The sidewalls of etched features, are subject to little or no bombardment. As a result, an anisotropic etch is realized, which is a desirable characteristic for the mainstream semiconductor industry where fine feature control is required.

When O_2 is added to CF_4, more F is available. This is because that the gas phase oxidation of CF_x accelerates CF_x dissociating into CO + F. Adding H_2 results in the formation of CF_2 and derivatives that cause thin CF_x films to form on surfaces and etch SiO_2 in the presence of ion bombardment. The etch rate of SiO_2 remains nearly constant for the concentration of H_2 up to 40 %, but the etch rate of Si by CF_4 gas decreases monotonically to almost zero when the H_2 concentration level reaches over 40 %. Adding too much H ($\geq$ 40%) causes a thick plasma polymer to coat all surfaces and reduces the etch rate until it stops; adding too much O_2 ($\geq$ 20%) dilutes the F concentration, and causes the etch rate to decrease. This model holds for other flourine-based gases, such as CHF_3, NF_3, and XeF_2. As fresh CF_x radicals are added from the gas phase, material in this carbonaceous layer is continuously gasified by the ion-induced sputtering and reaction with the SiO_2 film. Example reactions [53] are shown in Figure 2-7. Furthermore, it is believed

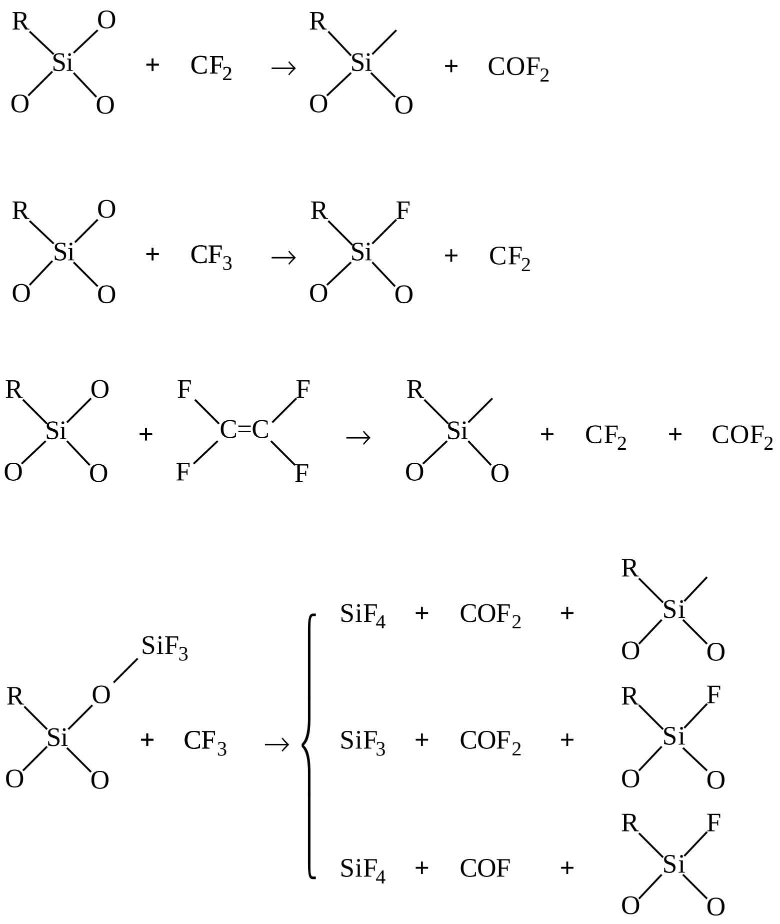


Figure. 2-7. **Typical reactions in the etch of SiO_2 with CF_x radicals, where R denotes F, O, or bound fluorocarbon chains (C_xF_y) and reactants shown (CF_2, CF_3, C_2F_4) represent classes of functional groups in the fluorocarbon layer[51].**

that CF_x and other fluorocarbon are first chemisorbed on a surface, then are dissociated. Less residue accumulates on SiO_2 surface because some carbon atoms combine with the oxygen in the SiO_2 to form CO and CO_2, which are volatile. However, there are no reactions with Si that can gasify the carbonaceous film when a high concentration of H_2 is added or a different gas is used, such as CHF_3, because the lack of oxygen in the Si substrate and a fairly thick layer accumulating on the surface block any further attack by sputtering and chemical etching. Thus, it turns out that the SiO_2 layer can be continuously etched under conditions while etching of the Si has ceased. Nevertheless, if the deposition rate of the carbon residue becomes too high, etching eventually stops on all surfaces in the chamber, including SiO_2 surface.

The aforementioned etching mechanism explains two observations discussed later in this thesis:

- Most sub-micron CMOS technologies contain Ti/W/N or Ta/N as a barrier/anti-reflection coating (ARC) layer. The etch rates of these materials in the flourine-based plasma are much higher than those of dielectrics, therefore, a passivation film on sidewalls to block or reduce chemical etching of these barrier layers is required. CHF_3 based plasmas provide this passivtion and are is preferred in the post-CMOS dielectric etching rather than CF_4, although CHF_3 yields a lower etch rate and the selectivity of etching the oxide to the Si substrate is not necessary.
- In etching low-K dielectrics as used in Cu interconnects (discussed in Chapter 5), a higher O_2 flow rate is used. High level F concentration in the plasma causes a fast etch of the TaN barrier layers and results in delaminating MEMS structures.

2. 5 CHALLENGE IN THE PROCESS

There are dramatic differences in RIE of dielectrics for post-CMOS micromachining when compared with integrated-circuit (IC) processing [49][55].

- First, for definition of microstructures, it is preferred to have no selectivity in the vertical etch direction between different types of silicon dioxide, silicon nitride and Si, since the structural etch must go through a stack of various dielectric layers. It is desired to develop a recipe whose behavior can be described by a quantified mathematical model and which can be easily adapted to different dielectrics in different foundry processes, *e.g.* when IC fabrication move from SiO_2 to a low-K dielectric. The etch selectivity between these dielectrics and etch-resist mask materials, *e.g.* aluminum (Al) or copper (Cu), should be kept as high as possible.

- Second, RIE induced ion milling of mask layers is significant because of the extremely long etch time (more than 2 hours) required for etching thick dielectric layers. This milling of mask layers can cause the loss of the device critical dimension. However, the physical bombardment is required in the RIE process, especially for removing by-product inhibitor layers on the surface during the dielectric etch. As in IC processing, the directivity of etching is achieved in part by control of passivation on the sidewall[56]. But too much polymerization on the surface will slow down the etching and limit the smallest spacing that can be achieved; too little polymerization will not provide protection on the sidewall, causing the loss of critical dimension of the dielectric underneath the mask.
- Third, electrical connection failures can result from the etch, mostly at vias which connect different metal layers. The failure rate is much higher for non-plug style vias. Failures are caused by two mechanisms as shown in Figure 2-8: one is the milling of the metal layer at corners of vias which results in an open circuit at the sidewall of vias, as in Figure 2-8(b). This is a physical bombardment dominant effect. The second is lateral etching of barrier/ARC layers which exist above and below each Al or Cu layer in sub-micron CMOS processes, and this is a chemical

dominant effect, as in Figure 2-8(c). With the tungsten plug vias or Cu filled vias, the rate of first failure mechanism can be significantly reduced. However, with ever increasing stacked height of sub-micron processes and higher aspect-ratio MEMS structures, a longer etch time is required, increasing the chance of chemical attack of barrier/ARC layers. This chemical etch of barrier/ARC layers can cause delamination of mechanical structures and lost of via contacts.

2. 5. 1 Complexity of RIE System

It is well known that plasma systems have a lot of processing variables, such as gas mixture, gas flow rate, pressure, radio frequency (RF) power, electrode spacing, electrode temperature, electrode material, the total area on the wafer being etched (loading) and previous processing steps. All these variables affect the requirements mentioned above and their influence is non-linear and correlated. Up to now there is no single physical model to completely describe the RIE process, especially when it is tailored for post-CMOS micromachining. The construction of a mathematical model, which quantitatively represents process responses as functions of the process variables, is practical, highly desirable, and permits the identification of optimized settings to satisfy all different requirements.

The problem of RIE etch of microstructures is illustrated in Figure 2-9. Multiple effects of RIE need to be optimized at the same time. Important effects include etch rate, loss of critical dimensions, survival of electrical connections and generation of polymers (on the sidewall and in the field). Most of times, these requirements conflict with each other. For example, to increase etch rate, the generation of passivation need to be reduced. This can be done by increase the RF power resulting in higher DC bias. But

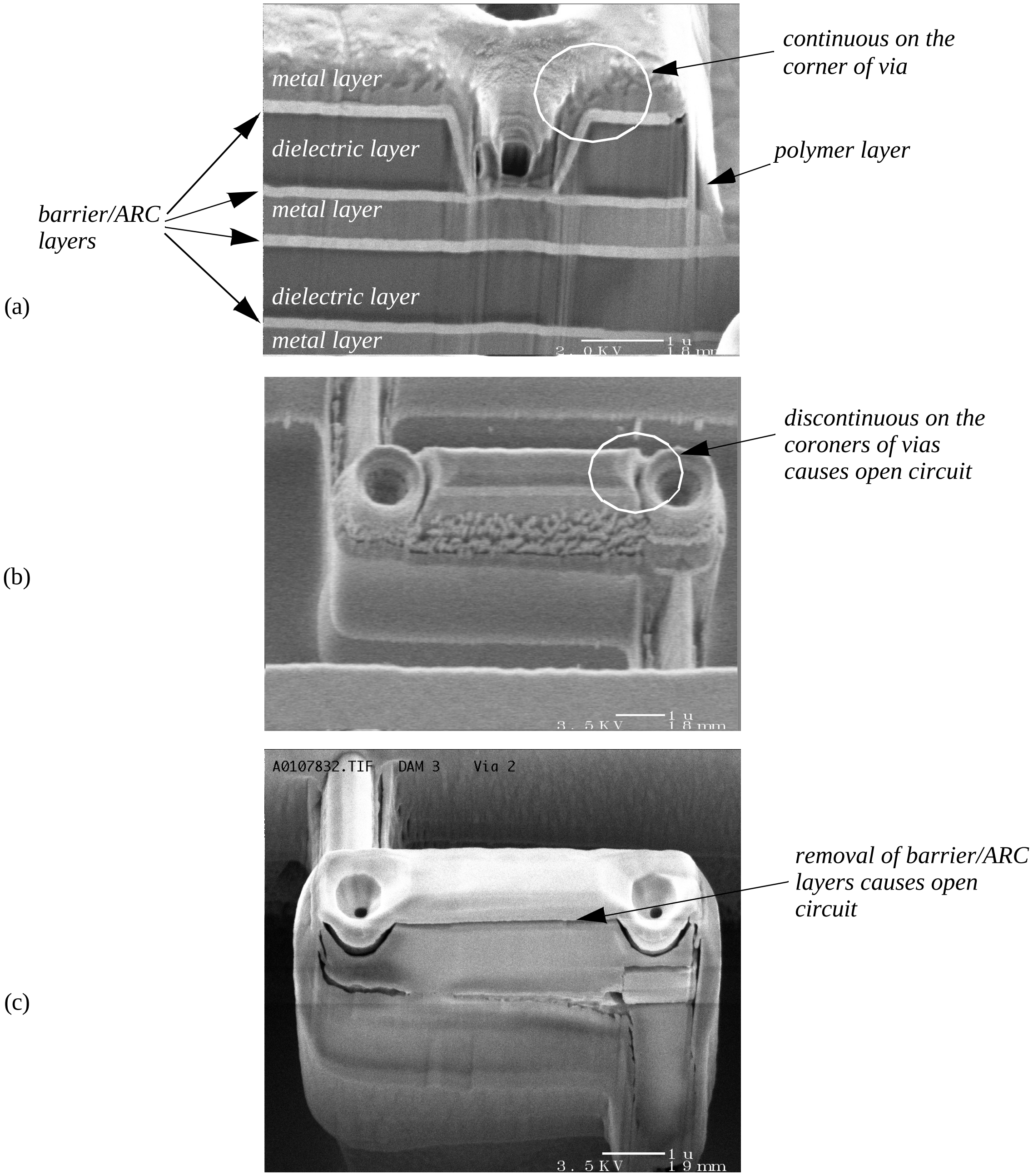

metal layer
dielectric layer
metal layer
dielectric layer
metal layer
barrier/ARC layers
continuous on the corner of via
polymer layer
(a)
2.0KV 1.8mm 1u
discontinuous on the coroners of vias causes open circuit
(b)
3.5KV 1.8mm 1u
A0107832.TIF DAM 3 Via 2
removal of barrier/ARC layers causes open circuit
(c)
3.5KV 1.9mm 1u

Figure. 2-8. **Via failure mechanism:**
(a) A via survives after the entire process flow,
(b) Physical effects dominate failure mechanism, loss of critical dimension and loss of corners on the vias by ion milling,
(c) Chemical effects dominate failure mechanism, lateral etch of barrier/ARC layers illustrated by FIB cross-cut of structures.

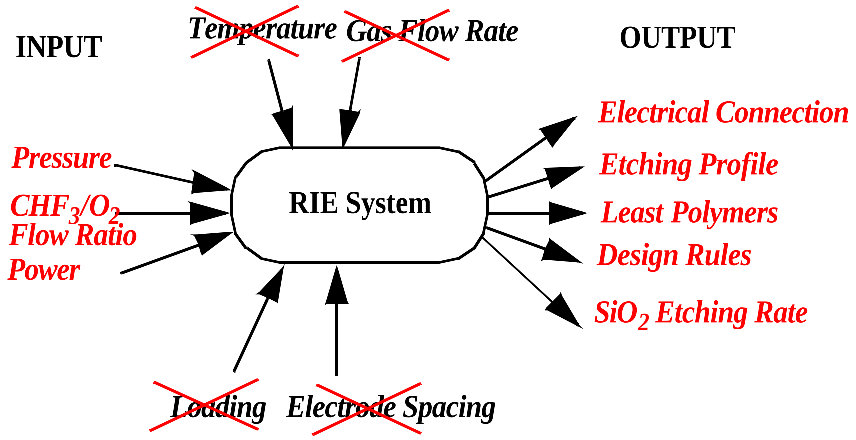

INPUT
~~Temperature~~
~~Gas Flow Rate~~
OUTPUT
Pressure
CHF_3/O_2 Flow Ratio
Power
RIE System
~~Loading~~
~~Electrode~~ Spacing
Electrical Connection
Etching Profile
Least Polymers
Design Rules
SiO_2 Etching Rate

Figure. 2-9. **Multiple responses of the RIE system as a function of multiple processing variables.**

increasing the RF power will cause the loss of the mechanical structure dimensions and the electrical connection failure. As in Figure 2-9, even the simplest parallel-plate RIE system has seven process parameters that can be adjusted. To ease the task, instead of exploring every combination of parameters, three major processing variables (pressure, power and mixture of gases) are chosen as experimental factors in a Box-Behnken factorial experiment [49][51][57] to generate different response surfaces. Detailed discussion of this method can be found in literature [61]. After a series of screening experiments, a CHF_3/O_2 mixture is chosen instead of the CF_4/O_2 mixture widely use for SiO_2 etch [51] as it generates sufficient passivation with a reasonable etch rate and less failure of electrical connection. The etching profile is evaluated by measuring the top metal layer thickness and line width after the dielectric etching as shown in Figure 2-10.

The starting point for the three processing factors was obtained from the manufacturer's recommended recipe and our prior experiments [31]. The space for conducting fac-

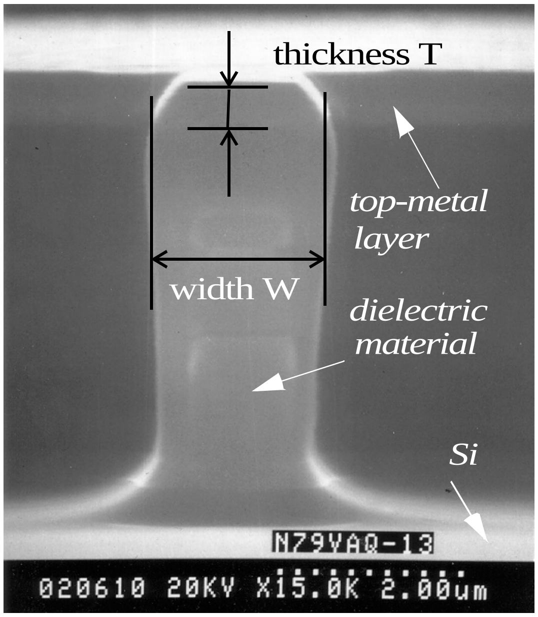


Figure. 2-10. **SEM of the cross section of a CMOS-micromachined beam's profile.**

torial experiments was determined by another set of screening experiments.

2. 5. 2 Response Surface Methodology

The benefit of Response Surface Methodology, a statistical technique, is that the experimental strategy and data analysis are combined efficiently to generate a parametric model that represents the process response. After the response has been quantitatively modeled, graphical representation of the response surface is generated in the parametric space. The trend of individual response from changes in the processing factors can be predicted. From multiple response surfaces of the processing requirements, a process window which satisfies different criteria simultaneously is obtained.

The only constraint in this method is that the response must be represented as a continuous variable, which means the original data is either a continuous variable or can be converted to a continuous fashion. Etch rate, mask layer thickness and beam width are obvious continuous data. However, the polymerization and electrical continuity are non-continuous variables which are hard to set criteria for the response surface analysis. For the polymerization, a rough quantitative measurement is adopted, where values are fit into three categories: 1 for heavily polymerized, 0.5 ~ 0.75 for the medium case and 0 for no polymerization. This quantization procedure is done by SEM inspection with visual evaluation. The electrical connection, determined by the resistance of vias connecting different layers are either conducting with a two-wire contact resistance measurement of about 7 to 16 Ω, or open, indicated by infinite resistance. In order to convert this to a continuous variable, an open-circuit is approximated by a 1 MΩ value of resistance. This value is large enough to establish the parametric model. Unfortunately, the intermediate value of contact resistance has not been observed, which implies the chemical reaction of barrier/ARC layer (titanium and tungsten compound in Agilent 0.5 μm process) with F^+ base plasma is extremely fast.

Attention should be paid to whether the particular process conditions being analyzed lead to instabilities which cause abrupt change in the response and are hard to model with continuous variables. Such conditions are typically avoided for desired operation because of their uncontrollable nature. Fortunately, these conditions have not shown up in our range of interest. Hence, the smooth and continuous regions of interest can be extrapolated and modeled by polynomial functions. The creation of polynomial expressions for each response as a function of experimental factors permits consideration of the trade-offs involved in process optimization. Carefully selecting the experimental design space will permit efficient model evaluation.

The effect of experimental error on the validity of a parametric model can be assessed using statistical analysis. First, the experimental error can be estimated by repeating experimental runs and calculating the standard deviation of the replicate differences. Also, the lack-of-model-fit can be estimated by performing extra trials to calculating the deviation between the model and the experimental data. The sum of these errors is called residual error; the difference between the number of data points and the number of model coefficients is called the degrees of freedom associated with the residual error.

2. 6 RESPONSE SURFACE DESIGN

In general, a response surface design should be chosen that will support at least a full quadratic model. Three levels of the various factors are needed for a quadratic model. The general form of the full quadratic model, which includes a constant term, *n* linear terms, *n(n-1)/2* two-factor interaction terms, and *n* quadratic terms for curvature, is:

$$Y = b_0 + \sum_{i=1}^{n} b_i X_i + \sum_{i=1}^{n-1} \sum_{j=i+1}^{n} b_{ij} X_i X_j + \sum_{i=1}^{n} b_{ii} X_i^2 \tag{2.1}$$

where Y is the process response and the X_i are the process variables. The three levels of X_i should be equally spaced on same scale (*e.g.*, linear, log, or square root). Thus for three factors, ten coefficients must be determined, and Eq. (2.1) can be simplified to:

$$\begin{aligned} Y = {} & b_0 + b_1 X_1 + b_2 X_2 + b_3 X_3 + b_{12} X_1 X_2 + b_{13} X_1 X_3 \\ & + b_{23} X_2 X_3 + b_{11} X_1^2 + b_{22} X_2^2 + b_{33} X_3^2 \end{aligned} \tag{2.2}$$

Following common practice, five extra trials are added to estimate residual error. A large number of data points gives better error estimation and model fitting; however, this leads to more consumption of time and effort.

The response function Eq. (2.2) can be solved by linear least-squares method when it is transformed to:

$$\eta = \theta_1 z_1 + \theta_2 z_2 + \ldots + \theta_{10} z_{10} \tag{2.3}$$

and the relations between the observation Y and the response function η can be expressed as:

$$Y = \eta + \varepsilon \tag{2.4}$$

provided by setting:

$$\begin{aligned} z_1 &= 1 \\ z_2 &= X_1 \\ &\ldots \\ z_5 &= X_1 X_2 \\ &\ldots \\ z_8 &= X_1^2 \\ &\ldots \end{aligned} \tag{2.5}$$

and

$$\begin{aligned} \theta_1 &= b_0 \\ \theta_2 &= b_1 \\ &\ldots \\ \theta_5 &= b_{12} \\ &\ldots \\ \theta_8 &= b_{11} \\ &\ldots \end{aligned} \tag{2.6}$$

Furthermore, by using the linear least-squares method, any response function can be transformed to:

$$\eta = \theta_1 z_1 + \theta_2 z_2 + \ldots + \theta_p z_p \tag{2.7}$$

with experimental conditions (z_{1u}, z_{2u},..., z_{pu}), $u = 1,2,...n$, have been run, yield observations Y_1, Y_2,...,Y_n. Then the model relates the observations to the known z_{iu}'s and the unknown θ_i's by n equations:

$$\begin{aligned} Y_1 &= \theta_1 z_{11} + \theta_2 z_{21} + \ldots + \theta_p z_{p1} + \varepsilon_1 \\ Y_2 &= \theta_1 z_{12} + \theta_2 z_{22} + \ldots + \theta_p z_{p2} + \varepsilon_2 \\ \ldots \\ Y_n &= \theta_1 z_{1n} + \theta_2 z_{2n} + \ldots + \theta_p z_{pn} + \varepsilon_n \end{aligned} \tag{2.8}$$

These equations can be written in a matrix form as:

$$Y = Z\theta + \varepsilon \tag{2.9}$$

where

$$\underset{n \times 1}{Y = \begin{bmatrix} Y_1 \\ Y_2 \\ \cdot \\ \cdot \\ \cdot \\ Y_n \end{bmatrix}}, \tag{2.10}$$

$$Z = \underset{n \times p}{\begin{bmatrix} z_{11} & z_{21} & \cdot & \cdot & \cdot & z_{p1} \\ z_{12} & z_{22} & \cdot & \cdot & \cdot & z_{p2} \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot & \cdot \\ z_{1n} & z_{2n} & \cdot & \cdot & \cdot & z_{pn} \end{bmatrix}}, \tag{2.11}$$

$$\theta = \underset{p \times 1}{\begin{bmatrix} \theta_1 \\ \theta_2 \\ \cdot \\ \cdot \\ \cdot \\ \theta_n \end{bmatrix}}, \tag{2.12}$$

$$\varepsilon = \underset{n \times 1}{\begin{bmatrix} \varepsilon_1 \\ \varepsilon_2 \\ \cdot \\ \cdot \\ \cdot \\ \varepsilon_n \end{bmatrix}}, \tag{2.13}$$

The sum of squares function is:

$$\begin{aligned} S(\theta) &= \sum_{u=1}^{n} ((Y_u - \eta_u))^2 \\ &= (Y - Z\theta)'(Y - Z\theta) \end{aligned} \tag{2.14}$$

The least-squares estimates, $(\hat{\theta}_1, \hat{\theta}_2 \ldots, \hat{\theta}_p) = \hat{\theta}'$, which minimize *S(q)* are given by,

$$Z'Z\hat{\theta} = Z'Y \qquad \textbf{(2.15)}$$

which is solved to yield:

$$\hat{\theta} = (Z'Z)^{-1}Z'Y \qquad \textbf{(2.16)}$$

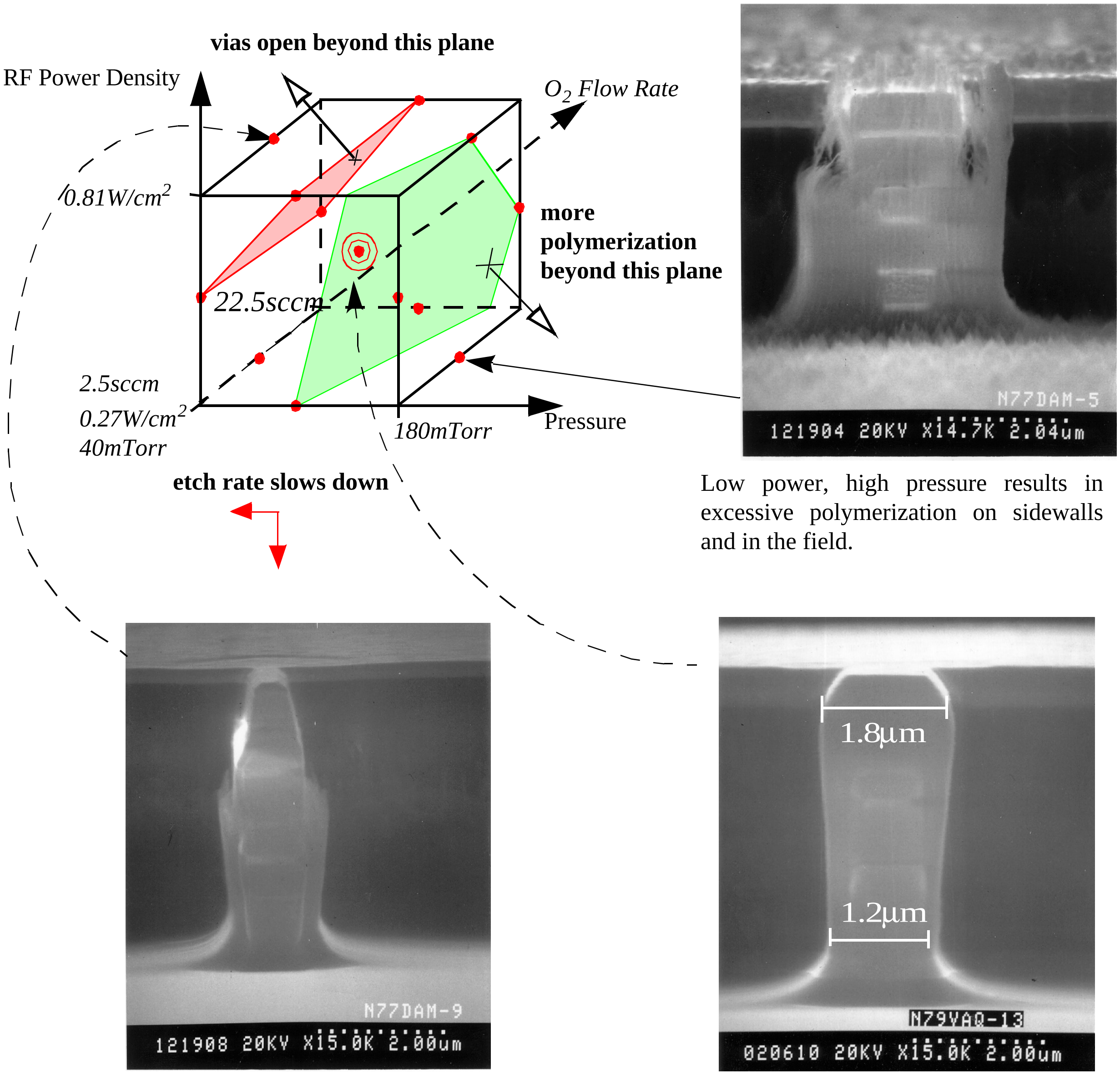
In our research, a Box-Behnken design [49][57][61] is chosen and it is illustrated in Figure 2-11 with fifteen trials for three-factor three-level experiments with twelve points on the each edge of the experimental space cube and two replicates at the center. The three levels of factors (power, pressure and O_2 flow rate) are shown in Table 2-2. Compared to a full-factorial design, twelve runs are saved out of twenty seven runs. The whole experiments was conducted on 2 mm × 2 mm chips from the Agilent 0.5 μm three-level Al interconnect SiO_2 dielectric CMOS process.

Table 2-2: **Levels of Three Factors in Box-Behnken Design of Experiments**

Factor	Low Level(-)	Middle Level(0)	High Level(+)
X_1 = Pressure (mTorr)	40	110	180
X_2 = Power (Watt)	50	100	150
X_3 = O_2 flow (sccm)	2.5	12.5	22.5

2. 7 EXPERIMENTAL RESULTS

The measured data from the factorial experiment is given in Table 2-3, where +/- and 0 correspond to the three-level settings of pressure, power and O_2 flow rate in Table 2-2. Figure 2-11 illustrates how the etch rate, electrical connection and polymerization varies with power, gas mixture and pressure. Etch rate is increased with increasing RF power and chamber pressure; it is not significantly affected by O_2 concentration. Increasing RF power and decreasing pressure cause a decrease in passivation. At high power levels, ion milling causes the top metal layer, Al in this case, to significantly thin down resulting in loss of critical dimension in the final microstructures. The ion milling can be compensated by increasing chamber pressure. The vias fail at process conditions of high power and low


vias open beyond this plane
RF Power Density
O_2 Flow Rate
0.81W/cm^2
more polymerization beyond this plane
22.5sccm
2.5sccm
0.27W/cm^2
40mTorr
180mTorr
Pressure
etch rate slows down
N77DAM-5
121904 20KV X14.7K 2.04um
N77DAM-9
121908 20KV X15.0K 2.00um
1.8μm
1.2μm
N79VAQ-13
020610 20KV X15.0K 2.00um

Low power, high pressure results in excessive polymerization on sidewalls and in the field.

High power, low pressure results in loss of critical dimension in the beam width.

The center point condition results in an adequate beam width and no polymerization with design line width = 2.1 μm.

Figure. 2-11. **The Box-Behnken three-factor design of experiment with constant CHF_3 flow rate at 22.5 sccm. The etch rate, polymerization and electrical connection vary with the processing parameters.**

Table 2-3: **Box-Behnken Design of Experiments for Dielectric Layer Etching**

Run No.	Pressure	Power	O_2 flow rate	Cal Etch Rate (*Å/min*)	Via contact (Ω)	Top Metal Layer Width (W) (*mm*)	Top Metal Layer Thick (T) (*mm*)	Polymer on Sidewall	Polymer in the field
1	+	+	0	663	16	1.800	0.582	0.00	0.5
2	+	-	0	127	16	1.680	0.625	1.00	1
3	+	0	+	373	7	1.868	0.636	0.50	1
4	-	-	0	120	12.0	1.585	0.381	0.00	0
5	0	-	+	145	7.8	1.843	0.598	0.50	0
6	-	+	0	311	100000	0.459	0.091	0.50	0
7	0	-	-	149	7.8	1.851	0.611	0.50	0
8	0	+	-	438	100000	1.171	0.372	0.50	0.5
9	+	0	-	336	8.6	1.852	0.587	0.75	1
10	0	0	0	353	11.5	1.748	0.508	0.00	0
11	-	0	+	214	12.6	1.331	0.191	0.00	0
12	0	+	+	462	100000	1.216	0.357	0.00	0
13	-	0	-	268	100000	1.150	0.309	0.00	0
14	0	0	0	375	9	1.822	0.500	0.00	0
15	0	0	0	377	9.5	1.822	0.512	0.00	0

pressure as shown in Figure 2-8.

The data generated by a response surface design is analyzed using Least Square Regression (LSR) analysis software from Minitab® [62]. The model coefficients are determined by minimizing the residual variances, as defined in Eq. (2.16). The coefficients of Eq. (2.2), with each factor normalized to ±1 and 0 levels, are listed in Table 2-4. The relative significance of each factor, their interactions and their quadratic effect can be extracted from the table. For example, increasing RF power increases the etch rate, and reduces the generation of polymer, especially on the sidewall. However, increased RF power also thins the top mask layer, reduces the beam width and is prone to cause via failure. Increasing pressure will mostly cause opposite effects. The interaction and quadratic

Table 2-4: **Normalized Coefficient Values for the Full Quadratic Model**

coefficient.	etch_rate (*Å*/min)	top metal layer width (μm)	to metal layer thickness(μm)	via contact (Ω)	polymer on the sidewall	polymer in the field
b_0	367.8	1.797	0.507	1070	0.000	0.000
b_1	70.3	0.319	0.178	-234000	0.223	0.438
b_2	161.6	-0.295	-0.101	371000	-0.127	0.000
b_3	-1.8	0.053	-0.008	-141000	-0.098	-0.063
b_{12}	-39.0	-0.170	-0.066	-17000	0.152	0.375
b_{13}	-33.7	-0.246	-0.021	265000	0.222	0.000
b_{23}	-35.6	-0.046	-0.002	233000	0.152	0.125
b_{11}	76.0	0.308	0.062	-242000	-0.371	-0.125
b_{22}	26.9	-0.072	0.033	283000	-0.055	0.000
b_{33}	7.5	0.033	0.000	-8000	-0.129	-0.125

coefficients have a significant effect on the responses. The interpretation of each factor's contribution to the final responses is quite difficult without assistance of graphic plots.

Figure 2-12 shows an example of an etch rate contour plot with the change of power and pressure and constant 16 sccm O_2 flow. The etch rate increases with power and pressure; and the etch rate is more insensitive to pressure at higher pressure level. By overlapping the contour plots generated with the upper and lower bounds of the desired responses as functions of the pressure, power and O_2 concentration, a set of acceptable processing parameters are derived, as shown in Figure 2-13. The central blank portion of the graph delimits the operating regime in which all criteria are met. The current processing point is at 125 mTorr chamber pressure, 0.55 W/cm^2, CHF_3 flow at 22.5 sccm and O_2 flow at 16 sccm. At the etch rate of 425 Å/min, it takes about 2 hrs to etch through all the dielectric layers in the Agilent 0.5 μm three-metal process. Previous recipes operated at a lower power level (about 0.27 W/cm^2), and took around 9 hrs to complete etching.

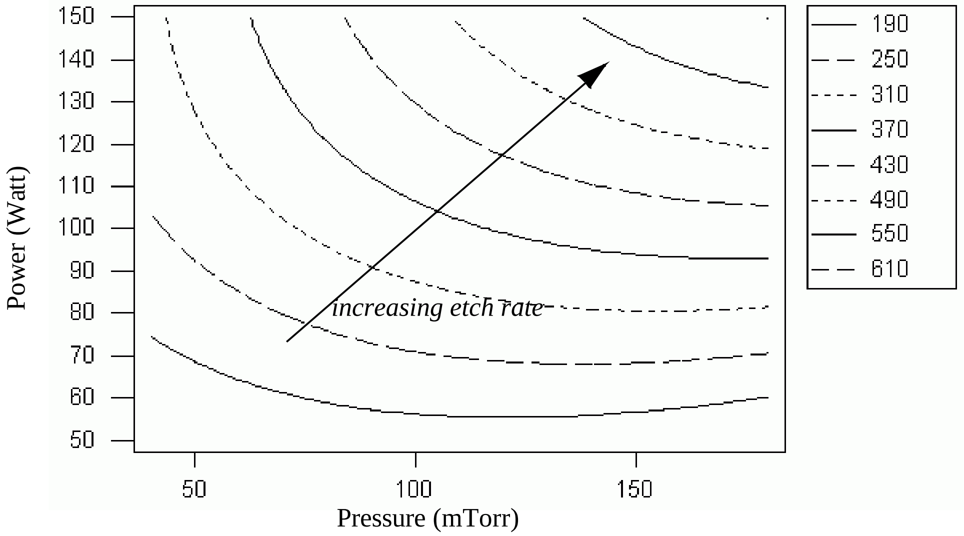


Figure. 2-12. **The etch rate (Å/min) contour plot as a function of power and pressure with 16 sccm of O_2 flow.**

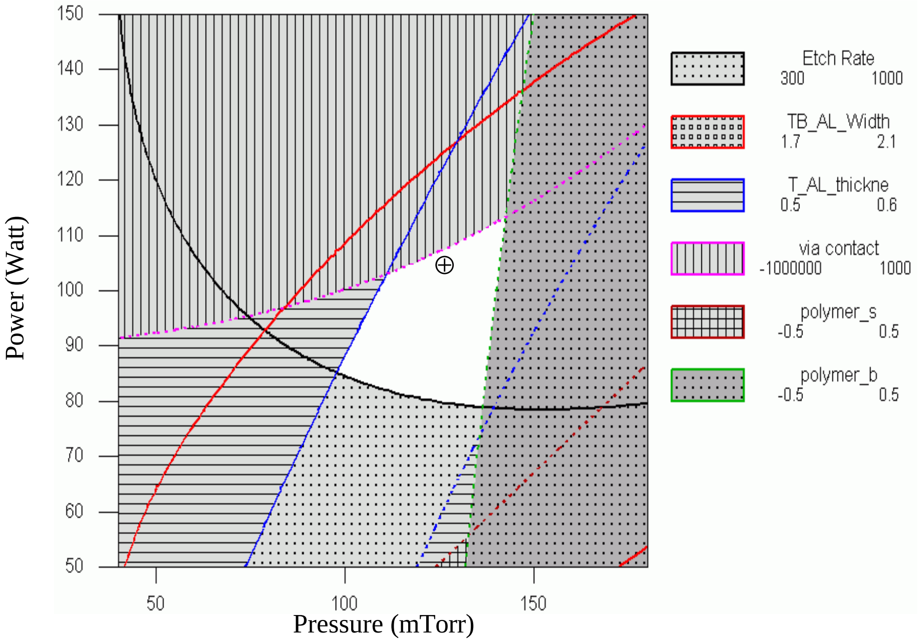


Figure. 2-13. **Overlay contour plots of etch rate, critical dimensions, electrical connectivity and polymerization with O_2 flow is held at constant 16 sccm, where Å indicates the current processing point.**

The quality of the model can be determined by examining by the *adjusted-R^2* number [57]. A perfect fit would have an *adjusted-R^2* value of 100%. The *adjusted-R^2* for the responses of etch rate, top metal layer width, top metal layer thickness, via contact, polymer on side-wall and polymer in the field are 97.8%, 95.3%, 97.9%, 72.5%, 85.6% and 78.4%, respectively. These values indicate that the quadratic parametric model represents dielectric layer etch rates, mask layer thickness reduction and loss of critical dimension of mask layer very well. The via contact, polymer on the side-wall and in the field are not represented as well by this model. For via connections, the model error is due to the abrupt change in the response. While for the polymer formation, the model error is due to the lack of the quantified criterion and accuracy in measuring the severeness of polymer formation. But in general, these results still give us good guidance on optimizing the process.

2. 8 DISCUSSION

2. 8. 1 The Effect of O_2 Concentration on Etch Rates

The O_2 concentration in the plasma reaction gas mildly affects the SiO_2 etch rate. As explained in Section 2. 4 and illustrated in Figure 2-14, when O_2 flow (< 10 sccm) is lower compared with feed gas, 22.5 sccm flow of CHF_3, less CHF_3 are disassociated and less F atoms are generated in the plasma; the combination rate of O with C is lower in the surface polymer layer, which forms violate CO and CO_2. Therefore, the SiO_2 etch rate reduces. On the other hand, higher O_2 flow (> 20 sccm) reduces the SiO_2 etch rate due to the dilution of the F concentration in the plasma.

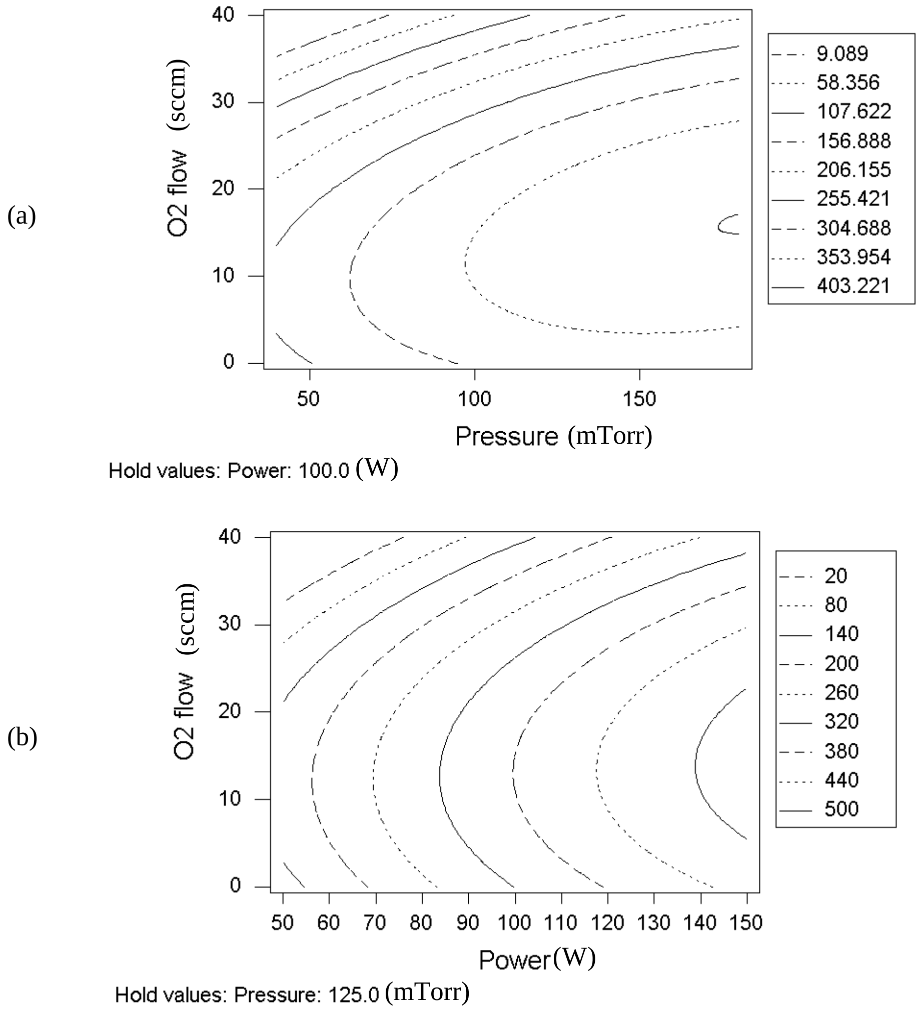
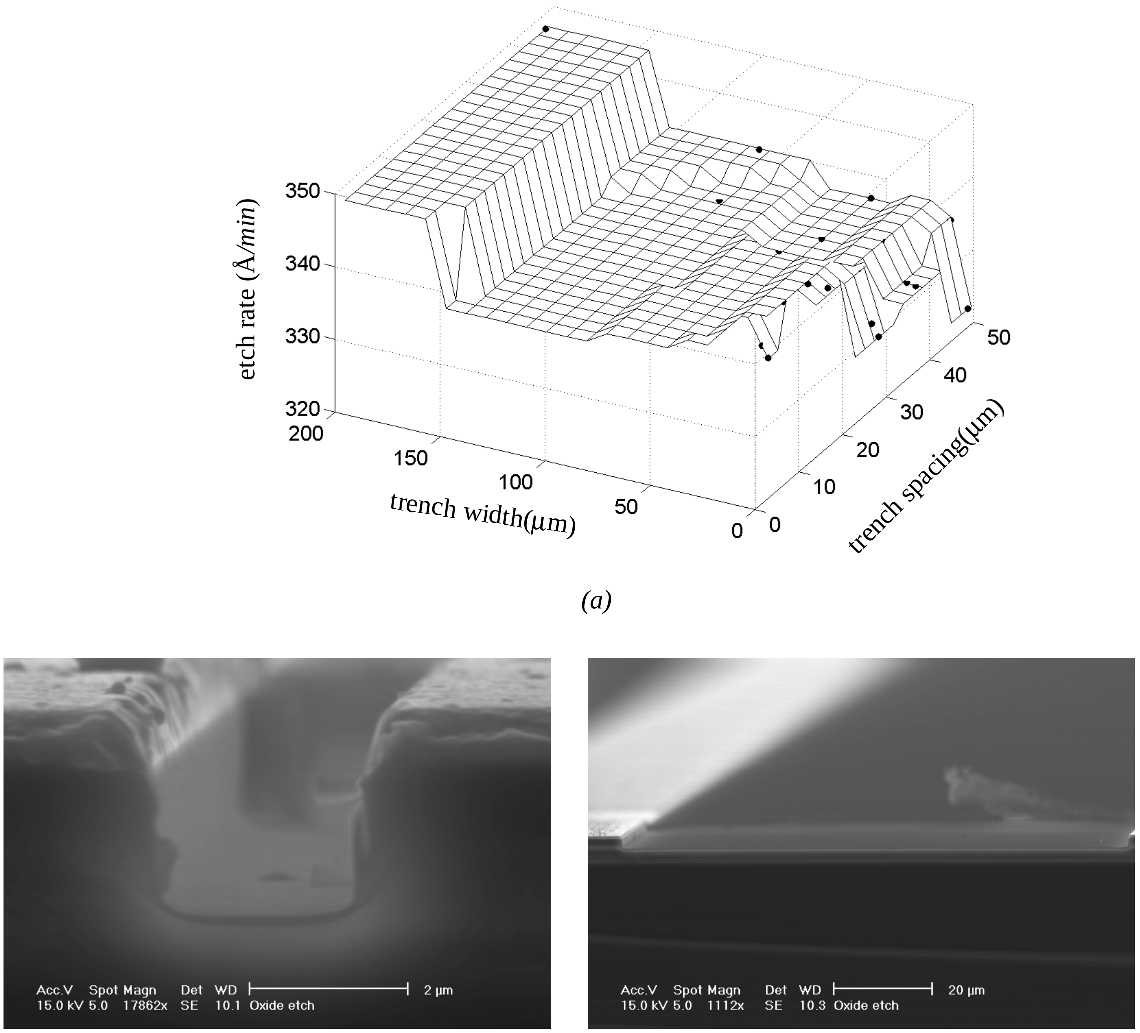


Figure. 2-14. The relation of SiO_2 etch rate (Å/min) and O_2 concentration in the gas flow.
(a) Contour plot of etch rate (Å/min) *vs.* O_2 flow and pressure, with fixed RF power.
(b) Contour plot of etch rate (Å/min) *vs.* O_2 flow and RF power, with fixed pressure.

2. 8. 2 Physical Mechanism in the Process

Based on current process parameters settings, the etch rates on a set of trenches with different combination of trench width and trench spacing are investigated. The experiment is done with process condition at 125 mTorr chamber pressure, 0.55 W/cm^2, CHF_3 flow at 22.5 sccm and O_2 flow at 16 sccm. When the etch does not go very deep (< 2 μm in this test), and maximum height to width ratio is less than 1:1, the etch rate variation is not very sensitive to the change of trench width and the density of trench. For example, the 2 µm wide trench etch in Figure 2-15(b) is compared with 100 µm wide trench etch in Figure 2-15(c). The 100 times increase in trench width only causes a 7.8 % increase in the etch rate.



(a)

(b) *(c)*

Figure. 2-15. **Etch rate variation with different combination of trench width and trench spacing for processing point is at 125 mTorr chamber pressure, 0.55 W/cm^2, CHF$_3$ flow at 22.5 sccm and O$_2$ flow at 16 sccm.**
(a) Surface plot of etch rate with different combination of trench width and trench spacing. The black dot represents the trench width and spacing combination being tested. The testing sample is 5 *m*m silicon dioxide with 1 mm Al wafer. The etch time is 60 min. The variation is less than 10%. Measured data are marked with solid black dots.
(b) SEM of 2 *m*m trench after etch.
(c) SEM of 100 *m*m trench after etch.

The increase in trench spacing doesn't have an obvious affect on etch rate. These are quite different from silicon etch processes discussed in later chapters and the later parts of this section. The geometric independence is due to two physical mechanisms dominating the etch. The first mechanism is that high energy impinging ions produce lattice damage at the surface being etched. At the damaged site, the increased reaction surface enhances the etch. The second mechanism, which is more important in SiO_2 etch, is that the energetic ions break the nonvolatile polymer layers (also referred to as surface inhibiting or blocking layers) that deposit on the surface being etched. The physical bombardment is the key characteristic in these two mechanisms. As illustrated in Figure 2-16, the direction of incident ions are not perpendicular to the etched surface, it has a distribution of the incident angle. For the height-aspect-ratio less than 2:1, there is no difference on etch rate between wide and narrow trenches. And there is no difference between the sparse and dense trench arrays. However, when the height-aspect-ratio becomes greater than 2:1, the size of the trench opening limits the number of ions that reach the bottom. It also limits the by-products of reaction being taken out of the trench, and consequently reduces the concentration of reactive radicals at the surface and reduces the etch rate.

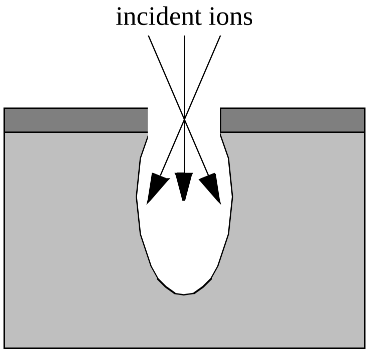


Figure. 2-16. **Angular distribution of incident ions.**

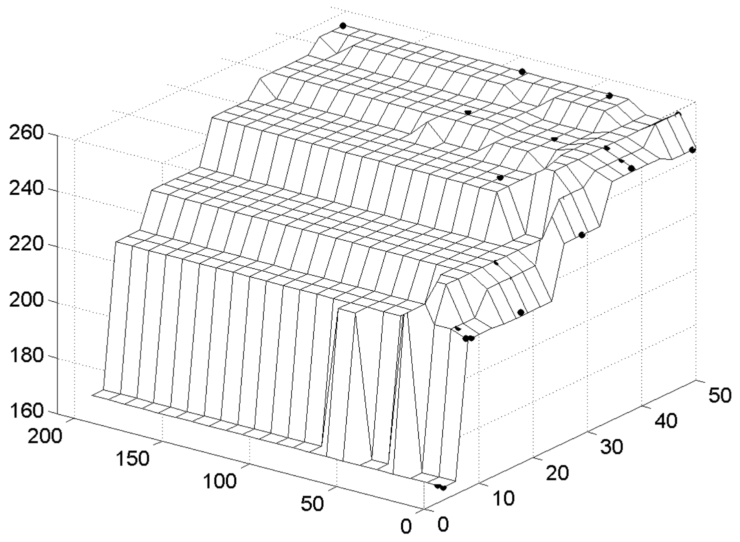


Figure. 2-17. **Etch rate variation with different combination of trench width and trench spacing for processing point is at 125 mTorr chamber pressure, 0.55 W/cm^2, CHF$_3$ flow at 22.5 sccm and O$_2$ flow at 5 sccm. Measured data are marked with black solid dots. Surface plot of etch rate with different combination of trench width and trench spacing. The black dot represents the trench width and spacing combination being tested. The testing sample is 5 *m*m silicon dioxide with 1 *m*m Al wafer.**

As illustrated in Figure 2-17, a 170 min etch was conducted on the same test pattern, as shown in Figure 2-15. The O$_2$ flow rate was set at 5.0 sccm such that photoresist can be used to cover most of the metal area during etching. The purpose of this photoresist mask layer is to reduce the micromasking effect that will be discussed in Chapter 5. The overall etch rate slows down as predicted in Figure 2-14. The higher aspect ratio contributes to not only the overall slower etch rate but also the significant etch lag. Comparing etch depth on a 2 µm trench with etch depth on a 200 µm trench, the etch lag is as high as 40 %; but the etch lag is less than 20% with 6 µm and 200 µm trench, where the high-aspect-ratio is less than 1. For most accurate characterization, the etch rate on different MEMS structures should be tested. However, due to the limitation of time and resources, only the etch depth of different trenches is observed. It is more efficient to check the overall etch lag effects after all process steps for other MEMS structures, as detailed in Chapter 3. To ensure the complete etch through dielectric layers with different openings, especially when considering comb finger structures with height-aspect-ratio over 2.5, 20 % or more over etch is recommended. Therefore, the height-aspect-ratio is limited to 2.8:1 in the design which corresponds to 1.8 μm spacing in the Agilent 0.5 μm CMOS process. A smaller spacing will dramatically increase the processing time, and induce more chances of failure categorized in former sections.

2. 8. 3 Chemical Mechanism in the Process

It is well known that the RIE is a plasma-enhanced chemical process, therefore, the concentration of reactive gas etchant in the chamber plays an important role in determining the etch rate of dielectric layers. As in Figure 2-12, increasing the chamber pressure, which increases the amount of etchant in the chamber, increases the etch rate. On the other hand, increasing RF power not only enhances the desorption of polymers on the etch front, a physical mechanism, but also increases the disassociation of reactive species from CHF_3, thus increasing the active radical concentration in the chamber. If a large continuous surface is to be etched, the etch rate dramatically drops down, well known as the loading effect. However, the pattern-factor-induced etchant concentration change on the etching surface is compensated by the plasma-related electrical-force-driven mass transportation instead of diffusion of radicals. Thus, a uniform etch can be achieved across the wafer but average etch rate is significantly affected by the chamber pressure, exposed area and flow rate when the chamber experiences a heavy etch load.

2. 9 SUMMARY

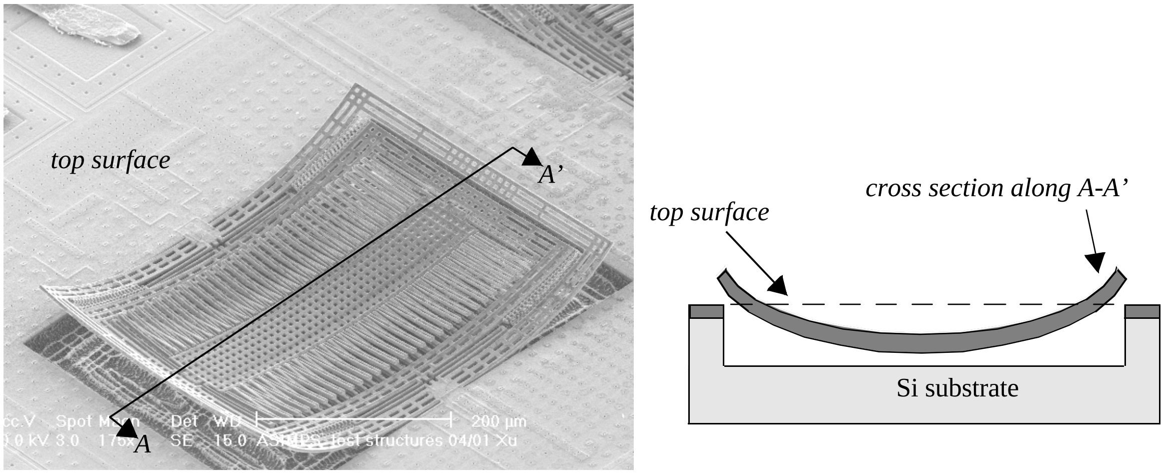
In this chapter, fundamentals of RIE have been highlighted in order to understand the process and challenges of RIE in the post-CMOS micromachining process. The Box-Behnken factorial experiment method, one of the robust and widely used design-of-experiment methods, is selected to optimize processing conditions of RIE etching of dielectric layers. A quantitative parametric model to represent this process has been obtained. The processing region for achieving minimal lateral etch, minimal polymerization and electrical continuity of vias has been determined. The factorial experiment design and the use of overlay contour plots dramatically reduced the time and effort to optimize this complicated processing. These results show that a systematic experimental approach is effective in process optimization. The second-order effects in the process optimization are also identified. The most important practical issue, etch lag, has been quantified. To alleviate processing difficulties, MEMS structure with height-aspect-ratio 2.8:1 or less is recommended.

3

Bulk Silicon Micromachining

3. 1 INTRODUCTION

In post-CMOS micromachining, the dielectric structural etch is followed by a Si release etch. The original release etch recipe used parallel-plate RIE isotropic Si RIE, due to the available processing capability at that time [29]. Although the concept was successfully demonstrated, major design considerations existed. Because of different residual stress in different layers of metal-dielectric composite structures, structures curl after release. For devices with anchors on opposite ends, such as accelerometers and gyroscopes, the corners of devices curl above the plane, and the center part of structures curl down [57], as shown in Figure 3-1. In severe cases, the proof mass may touch the silicon substrate, which inhibits its movement. Moreover, to reduce capacitive coupling from the substrate to the sensor, the separation between the sensor and substrate should be maximized. However the isotropic etch time to release microstructure from the substrate can not exceed a certain limit for two primary reasons. First, the etch step in Figure 1-1(c) is almost isotropic with vertical to lateral ratio about 2:1, circuitry must be put far away from the edge of the etch-resist mask in order to prevent being etched away during this step,


top surface
A'
A
200 µm
top surface
cross section along A-A'
Si substrate

(a) (b)

Figure. 3-1. **CMOS-MEMS accelerometer(design courtesy of H. Luo).**
(a) SEM shows excessive curling from Z-axis stress gradient in the metal-dielectric microstructure.
(b) Illustration of the center part of device (along A-A') curling down to the substrate.

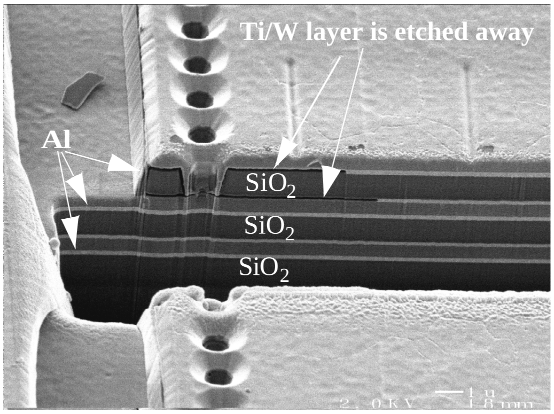

Ti/W layer is etched away
Al
SiO_2
SiO_2
SiO_2

Figure. 3-2. **Focus ion beam cross cut of CMOS microstructures shows that the Ti/W barrier/ARC layer is etched after Si isotropic etch by the SF_6/O_2 plasma. The bright thin layers are Ti/W barrier/ARC layers.**

especially when a large separation between the MEMS structure and the substrate is required. The extra spacing from the sensor to the circuitry increases the parasitic capacitance on the input nodes of the sensing circuitry. It can also comprise the effectiveness of anchors to structures due to slight curling from the undercut region. Second, it has been found that SF_6 can quickly etch Ti/W barrier/ARC layers [53], as shown in Figure 3-2.

This effect is similar to the failure mechanism in Figure 2-8(c) due to F^+ riched plasma. However, the etch of Ti/W is faster in SF_6 plasma than that in the CHF_3/O_2 gas mixture, because almost no polymer layer has formed as a passivation layer on the sidewall. In a parallel-plate RIE system, usually a 20 min Si isotropic etch is required to release general MEMS structures, *e.g.* 25 μm width beam with 20 μm etch pit surrounded. The extended etch can cause electrical contacts to be etched and mechanical structures to delaminate. This failure mechanism is strongly related to the chemical reactions of plasma to the surface. Except for timing the process or changing the reaction chemistry, nothing can prevent this failure from happening with parallel-plate RIE.

To overcome these difficulties, a new process flow is developed, as illustrated in Figure 3-3. The key feature is introducing an inductively coupled plasma (ICP) RIE for the microstructure release step, as in Figure 3-3(d). The thin-film dielectric etch step (Figure 3-3(a) and (b)) remains the same regardless of the choice of Si release etch processes.

Integrating the Bosch Si Deep RIE(DRIE) technique [60] into the process flow (Figure 3-3(c)) with a subsequent Si isotropic etch substantially decouples the vertical etch and lateral etch. The air-gap separation between microstructures and the substrate is primarily set by the Si anisotropic etch. The amount of the lateral etch required to release microstructures is determined by the isotropic etch.

The passivation step in the Si DRIE process deposits a thin layer of polymer on sidewalls of microstructures. This thin passivation layer significantly reduces lateral etching

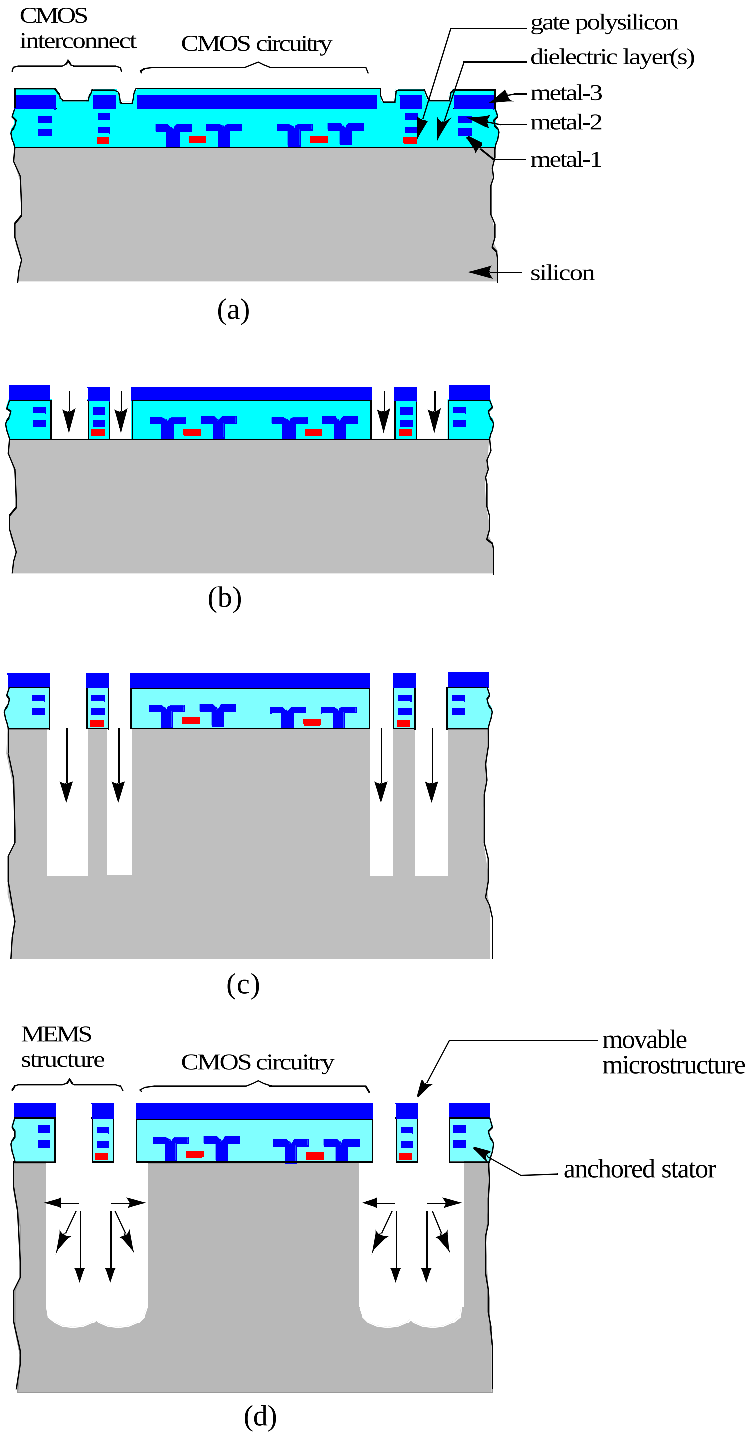

CMOS interconnect
CMOS circuitry
gate polysilicon
dielectric layer(s)
metal-3
metal-2
metal-1
silicon
(a)
(b)
(c)
MEMS structure
CMOS circuitry
movable microstructure
anchored stator
(d)

Figure. 3-3. **Cross sections in each stage of the process flow.**
(a) Device from a CMOS foundry service.
(b) Anisotropic etch of dielectric layer.
(c) Anisotropic etch of Si substrate.
(d) Isotropic etch of Si substrate to complete the process flow, resulting in integrated MEMS structures with CMOS circuitry.

of the Ti/W barrier/ARC layers by F^+ atoms. Therefore with the same undercut of Si, the yield of MEMS devices is much higher when they are processed in a DRIE system than in a traditional parallel-plate RIE system.

In this chapter, the physical and chemical mechanisms involved in the ICP RIE process are described. The configuration of a typical ICP system made by Surface Technology System (STS®) is illustrated as an example. Results of characterization of DRIE anisotropic and ICP isotropic etch of Si are described in following sections.

3. 2 ICP SYSTEM CONFIGURATION

An inductively coupled plasma (ICP) RIE system is an advanced RIE system, illustrated by system schematic in Figure 3-4. Compared with the parallel-plate system shown in Figure 2-4, the key feature in the ICP system is that the RF power required to generate radicals and the RF power required to etch the wafer can be separately controlled. As illustrated in Figure 3-4, the coil at the top part of the ceramic chamber provides the power to generate radicals, and the power source connected to the bottom electrode provides direction power for the directional etch. The self-DC bias on the wafer is controlled by this second RF source connected at the bottom. Usually the DC bias in the system is less than 100 V, whereas in a traditional RIE system, the bias of 300 V or higher is common. Therefore, in an ICP system, in order to increase the plasma density, more power can be delivered into the coil while the self-DC bias is not affected, and F^+ chemical etching of Si is enhanced, resulting in a high etch selectivity of the photoresist mask over the silicon. Ions spiral downward before they leave plasma instead of traveling straight down to the sub-

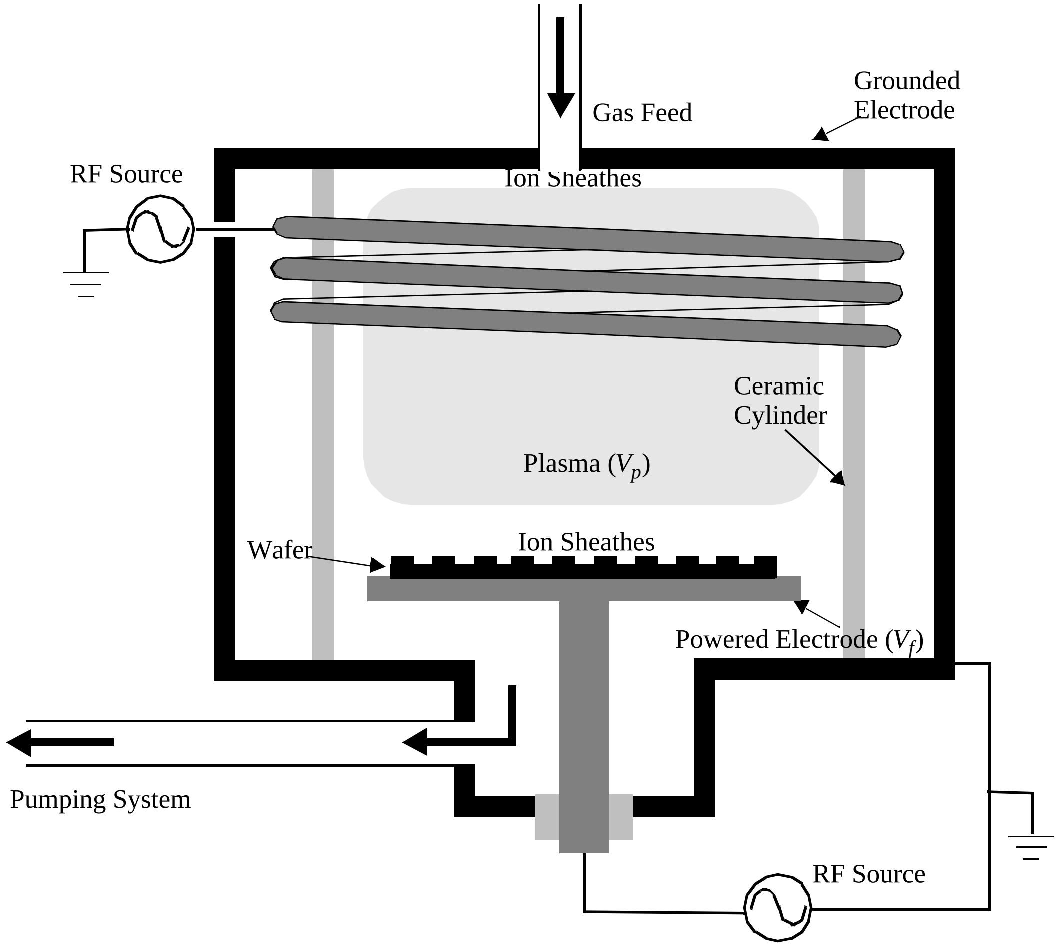

Gas Feed
Grounded Electrode
RF Source
Ion Sheathes
Ceramic Cylinder
Plasma (V_p)
Wafer
Ion Sheathes
Powered Electrode (V_f)
Pumping System
RF Source

Figure. 3-4. **A diagram of an ICP RIE system.**

strate. This is due to the existence of a magnetic field in the chamber. Ions travel a longer distance, have more collisions with other molecules, and generate more radicals for the etch. A typical processing pressure is between 1 mTorr to 100 mTorr and the plasma density is around $5 \times 10^{11}/\mathrm{cm}^2$, which is two orders of magnitude higher than a traditional RIE system. Because of high density of ion flux onto the surface, the wafer in the process has to be cooled and it is thermally contacted to the metal electrode by helium backside cooling to control the surface temperature. A high conductance vacuum system is usually required to reduce the residual time of numerous etch by-products in the chamber. Compared with a capacitively coupled plasma system and an electron cyclotron resonance (ECR) system, the ICP etcher is much simpler and the etch is more uniform across the wafer.

3. 3 SCREENING EXPERIMENTS

The very first experiments verify that the ICP system can be adopted into the post-CMOS micromachining process. Two questions must be answered:

- whether an Al metal mask can be used in the ICP chamber, at least at the die level;
- whether the Ti/W barrier/ARC layers will survive, or in another words, whether the structure will delaminate within the process window.

From the data collected, it is confirmed that Al films from CMOS foundries and MEMS foundries are very good etch masks in the ICP chamber, regardless of being sputtered or evaporated. Any decrement of Al layer thickness and critical dimension in this process within a useful etch time has not been observed. Although the ICP system generates a much higher density plasma than a conventional parallel-plate system, lower bias voltage significantly reduces the ion-milling effect of the Al mask even under a higher ion-flux condition. The experimentally measured etch rate of evaporated Al film in the ICP system is at 16 to 38 Å/hr with about 60 V self DC-bias. The large etch selectivity is a big advantage of a ICP RIE system over a common parallel-plate RIE system, where the Al mask layer thickness reduction is significant, about 0.3 μm/hr [58].

The Al mask commonly exhibit resputtering in RIE, causing “micromasking” and leading to “grass” in the field region. However, such micromasking effects in dice level are not observed. The micromasking effect at wafer level processing will be discussed in the later chapter.

The second observation is that there is no noticeable etching of Ti/W barrier/ARC layers within the Si isotropic etch process window. Preserving the Ti/W layers ensures that the mechanical structures do not delaminate and that electrical contacts between different metal layers survive after the release process. So the process yield is significantly increased and device reliability is assured.

3. 4 SI ANISOTROPIC ETCH

As described in Figure 3-3, an anisotropic process step is required in the process flow, and it is implemented in a STS Advanced Silicon Etching (ASE) DRIE system with a time multiplexed deep etching (TMDE) technique, which is licensed from the Bosch patent [60]. The fundamental aspect of this technique is the alternation of the passivation cycle, Figure 3-5(a), and the etching cycle, Figure 3-5(b), continuously during the process. In the STS ASE etch, the gas used for etching is SF_6/O_2 and the gas used for passivation is C_4F_8.

3. 4. 1 Si Etching Mechanisms

Typical physical and chemical reactions of the ASE process can be represented as the following reactions [61]. During etching cycles, ion and radical species are formed by electron impact dissociation:

$$SF_6+e^- \rightarrow S_xF_y + S_xF_y^* + F^* + e^- \tag{3.1}$$

$$O_2 + e^- \rightarrow O^+ + O^* + e^- \tag{3.2}$$

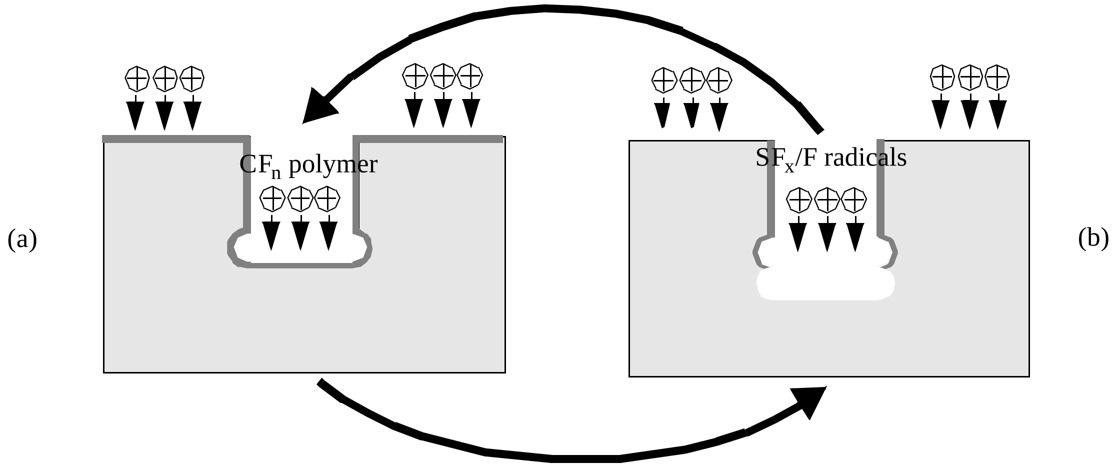


Figure. 3-5. **Basic concepts of the Bosch DRIE process.**
(a) The passivation cycle of the process. A CF_n polymer from the C_4F_8 plasma is deposited on all surfaces.
(b) The etching cycle of the process. The thin passivating film is first removed from the surfaces exposed to ion bombardment, then the exposed Si surface is isotropically etched by fluorine species from the plasma.

These relations neglect S_xF_y + O interactions, which act to decrease S_xF_y polymers and increase F radical formation, assuming the O concentration is not in saturation. The role of O is primarily to passivate the Si surface by reacting with Si and to adsorb onto the surface to form an oxide film:

$$O^* + Si_{(s)} \rightarrow Si_{(s)}\text{-}nO \rightarrow SiO_{n(sf)} \tag{3.3}$$

Where *(s)* and *(sf)* indices denote surface and surface film respectively. The surface passivation film them must be removed by the plasma prior to etching of the Si by the F:

$$SiO_{n(sf)} + F^* \rightarrow SiO_{n(sf)}\text{-}SF \tag{3.4}$$

$$SiO_{n(sf)}\text{-}F + \text{ion energy} \rightarrow SiF_{x(ads)} + SiO_xF_{y(ads)} \tag{3.5}$$

where the F adsorbs *(ads)* onto the surface, as in Reaction. (3.4), and ion bombardment removes the passivation film by enhancing the adsorption, reaction and desorption, as in

Reaction. (3.5). Then F radicals can proceed with silicon etching, which is one of the best understood and most widely used plasma process. When Si surface is exposed to atomic fluorine, a fluorinated “skin” quickly forms and extends about one to five mono-layers into the bulk Si substrate. Hence, when etching, F atoms penetrate into the fluorinated layers and attack subsurface Si-Si bonds and liberates two gaseous desorption products — the free radical SiF_2 and the stable end product SiF_4, as in Figure 3-6.

The SF_6 (or CF_4) is preferred over pure F_2 because of its lower toxicity. In the discharge, fluorosulfur radicals (S_xF_y) can react with free atoms and sometimes form poly-

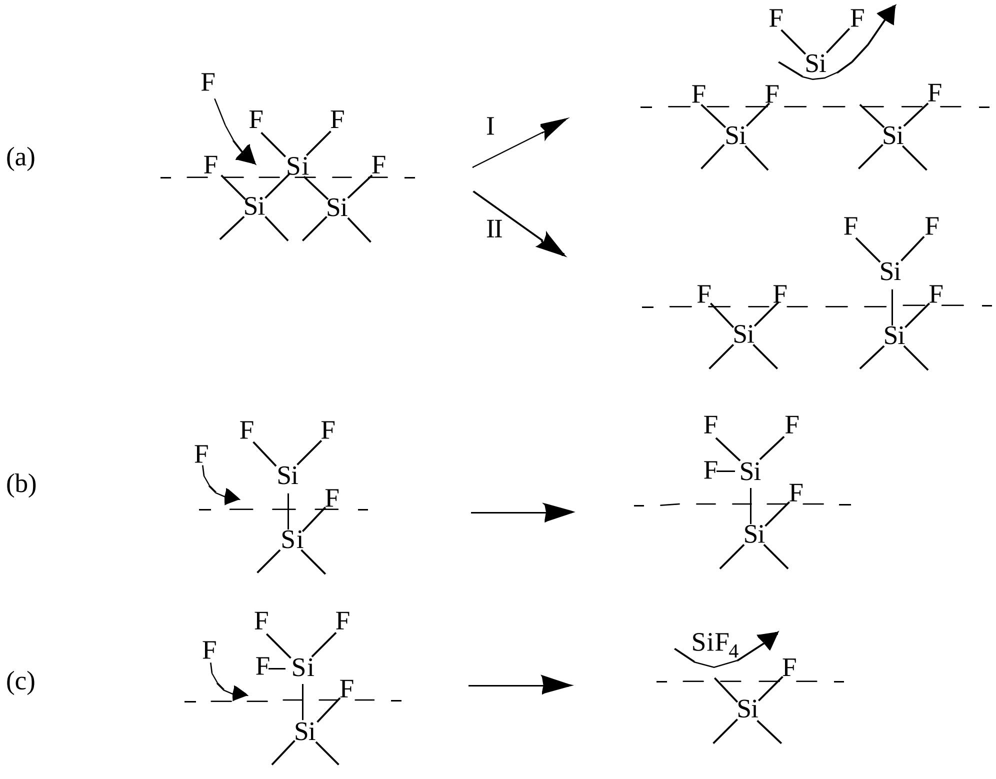


Figure. 3-6. **The isotropic etching mechanism of Si [49].**
The SiF_2 by-products are generated through channel I in (a)
The SiF_4 gaseous by-products are generated through channel II and (b), and go through a series of additions before desorbing as SiF_4 (c).

meric residues. In addition to oxidizing the surface as discussed above, O_2 added into the process also reacts with unsaturates making F atom, while depleting these polymer-forming species. However, too much O_2 addition dilutes the F concentration in the plasma and reduces the Si etch rate.

The physical bombardment of the surface also plays an important role in the Si isotropic etch. However, the bombardment is not critical when F atoms are saturated, and the etch proceeds chemically due to the volatility of the SiF_4. On the other hand, Reaction. (3.5) shows the critical role played by the ions in removing SiO_n films on the Si surface. The removal of SiO_xF_y also occurs as a result of either the physical sputtering or the by-products formation of SiF_x and SO_x after ion assisted reaction with S_xF_y. The passivation by O_2, its removal, and etching of the Si occurs simultaneously. In a high-aspect-ratio structural etch, a relatively high ion bombardment energy is necessary to completely remove the passivation layer, especially from the bottom of the structure. Incomplete removal of this passivation layer results in grass-like residues with the appearance of “black silicon” as the inevitable rough surface. The process flow in Figure 3-6 can be summarized in the following reactions:

$$\mathrm{Si} + \mathrm{F}^* \rightarrow \mathrm{Si\text{-}nF} \tag{3.6}$$
$$\mathrm{Si\text{-}nF} + \text{ion energy} \rightarrow \mathrm{SiF}_{x(ads)} \tag{3.7}$$
$$\mathrm{SiF}_{x(ads)} \rightarrow \mathrm{SiF}_{x(g)} \tag{3.8}$$

3. 4. 2 Passivation Mechanism

The deposition precursor gas, *e.g.* C_4F_8 in the STS ASE process, is dissociated by the plasma to form ions and radical species, which undergo polymerization reactions and result in the deposition of a polymeric layer:

$$C_4F_8 + e^- \rightarrow C_4F_x + C_4F_x^* + F^* + e^- \tag{3.9}$$

$$nC_4F_x^* \rightarrow nC_4F_{2(ads)} \rightarrow nC_4F_{2(f)} \tag{3.10}$$

This passivation layer $nC_4F_{2(f)}$ is deposited on surfaces of the silicon and the mask during the passivation cycle. In the etching cycle, the gas is switched to SF_6. The SF_6 first dissociates as in Reaction. (3.1). Then F radicals remove the surface passivation,

$$nC_4F_{2(f)} + F^* + \text{ion energy} \rightarrow C_4F_{x(ads)} \rightarrow C_4F_{x(g)} \tag{3.11}$$

before the Si etching can proceed as in Reaction. (3.4), Reaction. (3.5) and Reaction. (3.6). The directionality of the etch is controlled by the ion bombardment in its role of aiding the removal of the surface polymer.

3. 4. 3 Balance of Etching and Passivation

As discussed above, during the passivation cycle, fluorocarbon discharges contain a variety of radicals, which form Teflon-like films on all surfaces. During the subsequent etching cycle, passivation films are preferentially removed from surfaces perpendicular to the incoming ion/radical flux due to the ion bombardment; while surfaces parallel with the ion/radical flux experience much less impingement. Therefore, the passivation films prevent the etch of sidewalls by the radicals and F atoms. SF_6 discharges lack polymer-forming species to block the spontaneous etching, and the etch profile by F based species is almost isotropic. The anisotropic etch is achieved by precisely balancing the etch and the passivation. However, a scallop profile can be observed on the etched sidewalls, as in

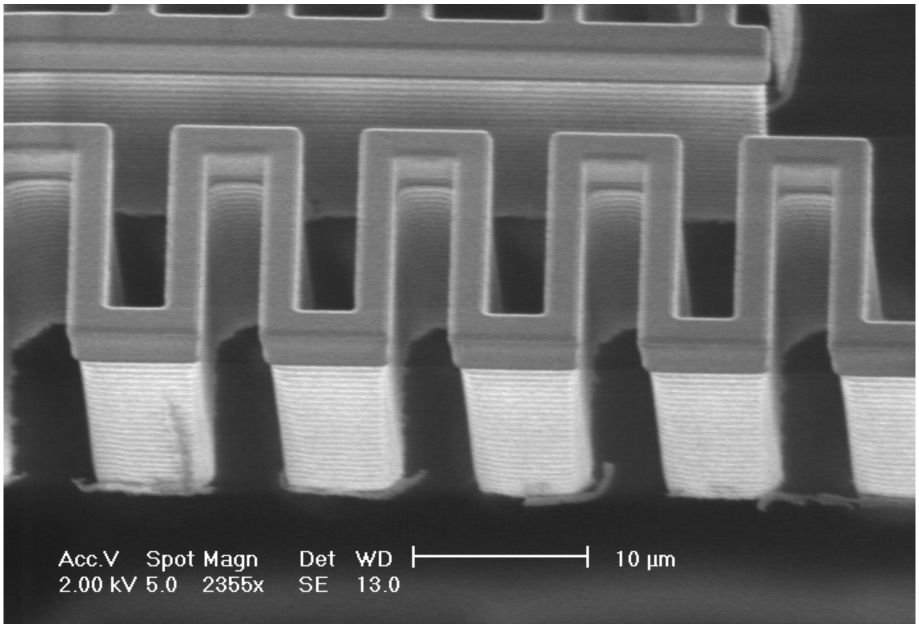


Figure. 3-7. **The scallops shown on the sidewall due to isotropic etch cycles.**

Figure 3-7. Depending on the roughness requirement, the amount of Si being etched during the etch cycle should be justified. A short etch cycle is usually used to achieve smooth sidewall, at the expense of a lower etch rate and longer process time.

3. 4. 4 Characterization of the DRIE process

Due to the capability of producing high-aspect-ratio structures, the DRIE process is well accepted in the MEMS community. Besides the process development effort from equipment manufactures [62], significant research efforts have also been invested from end users to characterize and optimize the DRIE process, both in universities [63][64][65] and in industry [66][67]. By balancing the etch and passivation, a variety of desired profiles can be achieved. A maximum 50:1 high-aspect-ratio deep trench etch has been reported [66][68].

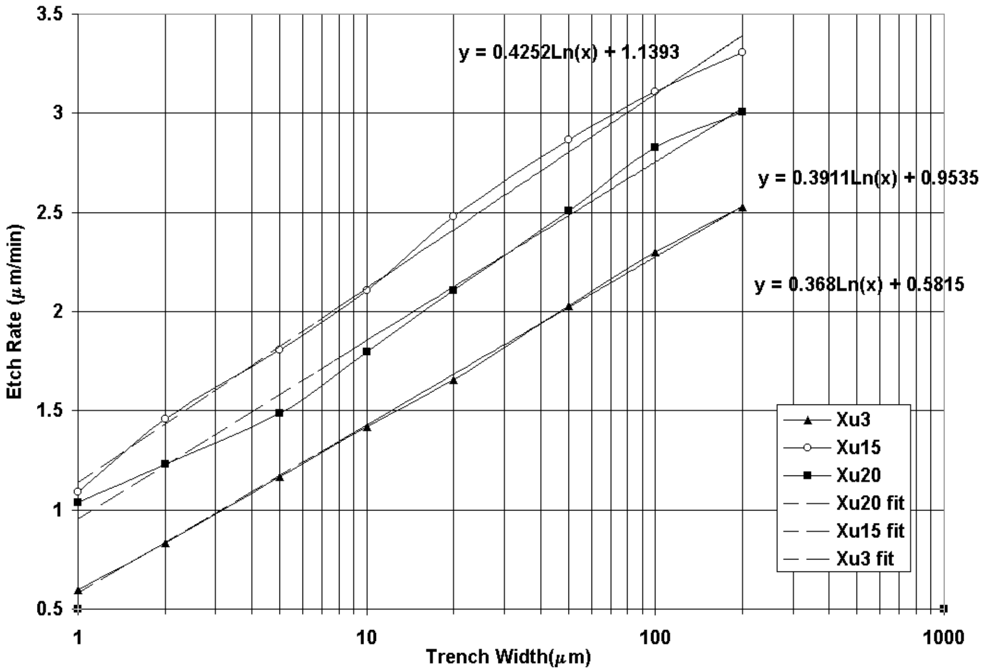


Figure. 3-8. **The measured etch lag effect in the DRIE anisotropic Si etch.**

In this work, the etch lag effect of DRIE etch is quantified, because it determines the processing time required for different MEMS device designs. As aforementioned, this processing time is determined by the amount of spacing from the structure to the substrate in order to allow for the residual stress-induced curling in CMOS-MEMS structures. In some applications, this spacing should also be large enough to reduce the capacitance between the substrate and the sensor. Figure 3-8 shows the etch lag effect in the DRIE anisotropic Si etch, the processing conditions are listed in Table 3-1. It shows the etch rate increases linearly with the logarithmic progression increasing of the trench width in different processing recipes. This etch lag effect can be explained by the standard vacuum theory. Very high-aspect-ratio structures decrease the conductance of the trench, and impedes both the transport of etchant species down to trench bottom and the removal of etching by-

Table 3-1: The Processing Parameters Used in DRIE Etch Lag Test

	Xu3	Xu15	Xu20
SF_6 Flow (sccm)	105.0	140.0	140.0
O_2 Flow (sccm)	10.5	0.0	0.0
Coil Power in Etch (W)	600.0	600.0	600.0
Platen Power in Etch (W)	12.0	12.0	16.0
Etch Time (sec)	15.0	15.0	16.0
Overrun in Etch (sec)	1.0	0.0	0.0
C_4F_8 Flow (sccm)	20.0	58.0	20.0
Coil Power in Passivation (W)	600.0	600.0	600.0
Platen power in passivation (W)	6.0	6.0	3.0
Passivation Time (sec)	11.0	6.00	6.0
Overrun (sec)	0.0	0.0	0.0
APC angle (%)	65.0	65.0	65.0
Processing time (min)	100.1	100.1	100.1

products [69][70][71][72]. This is called the theory of neutral flow conductance. As shown in Figure 3-9, the etch rate (normalize to 200 μm trench etch rates) decrease linearly with logarithmic increase of the height-to-width aspect-ratio. It is conclude that the etch rate decreases as the etch goes deeper into the substrate.

3. 5 SI ISOTROPIC ETCH

3. 5. 1 Screening Experiments

Figure 3-10 shows lateral etch depth *vs.* time for five runs of 4 mm^2 dice from the Agilent 0.5 μm CMOS process under conditions of 50 mT chamber pressure, 130 sccm SF_6 flow, 12 W platen power and 600 W coil power in a STS multiplex ICP chamber (installed in the Cronos facility). Lateral etch rate at the edge of the chips, is 4.08 ± 0.50 μm/min, which is relatively constant over the 4 min etch time investigated. The variation in etch rate comes from the procedure of ICP system to ramp up pressure

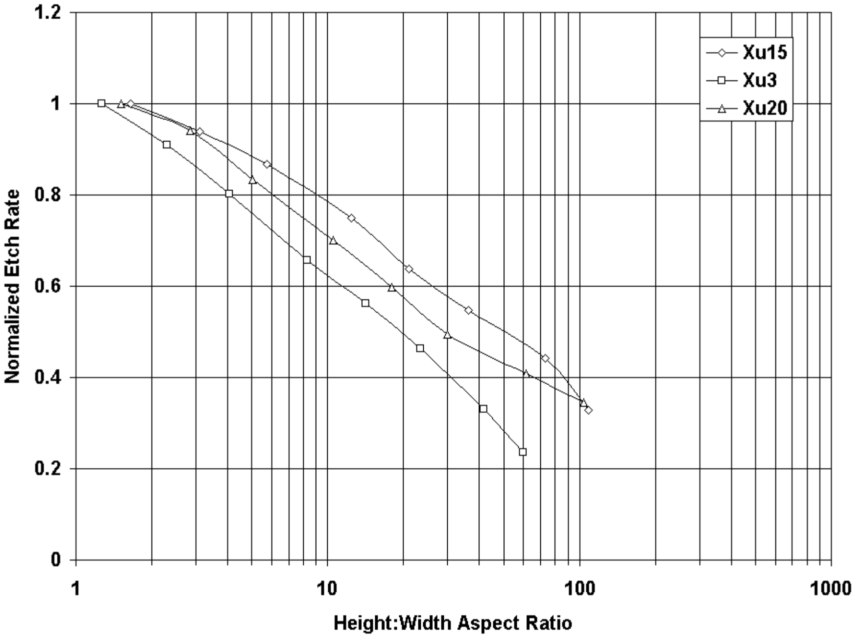


Figure. 3-9. **The etch lag effect in the DRIE anisotropic Si etch.**

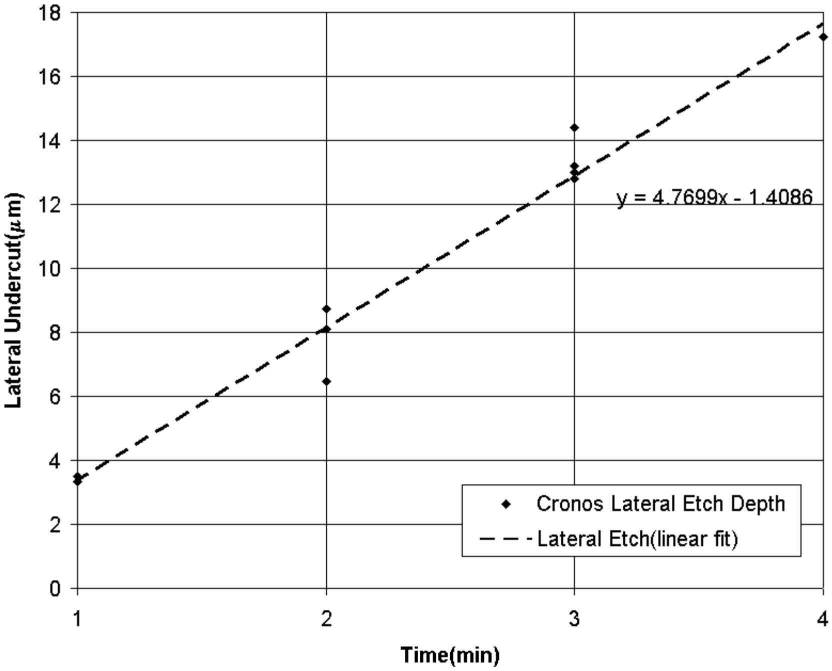


Figure. 3-10. **Lateral etch depth (*m*m) at the edge of chips as a function of time (min) for isotropic Si etch in an STS ICP system.**

and stabilize the plasma. When the processing time is greater than 3 min, the variation is reduced to 4.40 ± 0.20 μm/min.

3. 5. 2 Response Surface Design

An ICP plasma system has many process control variables and their effects on the process is very difficult to be modeled accurately. A mathematical model to quantitatively represent the etch response as a function of the process variables is required for Si etch process development. Response Surface Methodology (RSM) [55] has been applied to characterize the ICP system based on the previous successful experience with dielectric characterization.

With an assumption that the response surface can be represented as a full quadratic model, three levels of the various factors are needed for a quadratic model. With three factors, ten coefficients must be determined, as given in Eq. (2.2) in Chapter 2. Five extra trials are added to estimate the residual error. A large number of data points gives better error estimation and model fitting; however, this leads more consumption of the time and effort.

A Box-Behnken factorial experiment [55] has been applied to characterize the isotropic Si etch process in an STS ICP system with 4" wafers. Key mask features used in CMOS-MEMS structures are included. Experiments are conducted by varying three major processing parameters: the process pressure, the platen power and the SF_6 flow rate. Silicon dioxide is used as the etch mask. Under the assumption of a quadratic response model, fifteen trials for three-factor three-level experiments with twelve points on each edge of

Table 3-2: Three Levels of Three Factors

Factor	low-level(-)	mid-level(0)	high-level(+)
X1=Pressure (mT)	16	33	50
X2= Platen Power (W)	6	18	30
X3=SF_6 flow (sccm)	80	105	130

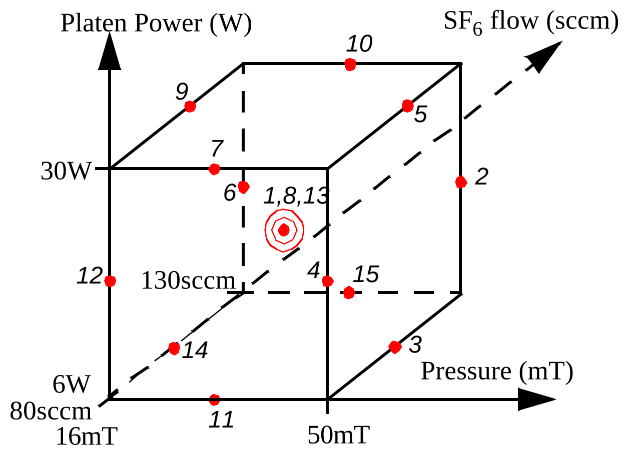
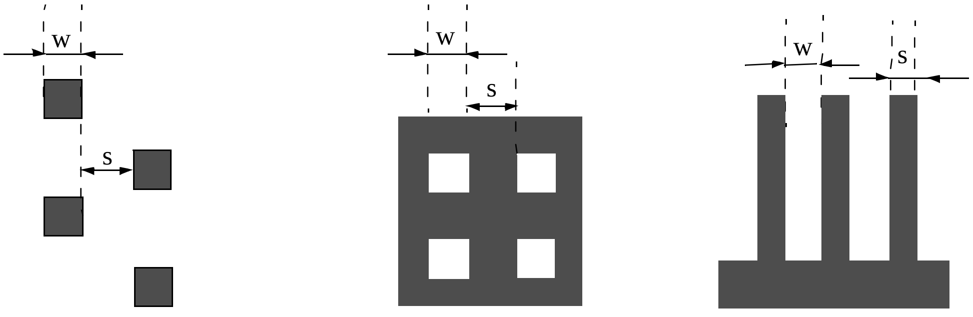


Figure. 3-11. The Box-Behnken three-factor design of experiment. The run numbers are labeled beside solid dots which indicate the processing parameter set-up.

the experimental space cube and three replicates at the center are required to determine the lateral etch response surface, as shown in Figure 3-11. The three levels for each factors are shown in Table 3-2. The total lateral etch time is 4 min. Compared to a full-factorial design, which requires twenty-seven runs, twelve runs are saved. The experiment covers the primary process space currently available for deep Si etching by the ICP system.

3. 5. 3 Experimental Results

The measured data on different patterns, as in Figure 3-12, from the factorial experiment are given in Figure 3-13 and Figure 3-14. These test patterns include squares with 1:1 and 1:5 spacing, cantilever beams with 1:1, 1:5 and 1:10 spacing as in Figure 3-13 and holes of 5 µm, 10 µm, 20 µm, 40 µm and 100 µm size with 1:5 spacing as in Figure 3-14.



(a) square

hole

cantilever beam

Figure. 3-12. **Test patterns include (a) squares, (b) holes and (c) cantilever beams. Their width or size (W) over spacing (S) ratio is equal to W:S. A special test structure, called "quick cleave" (qcleave), has a combination of 10 different beam widths with W:S = 1.**

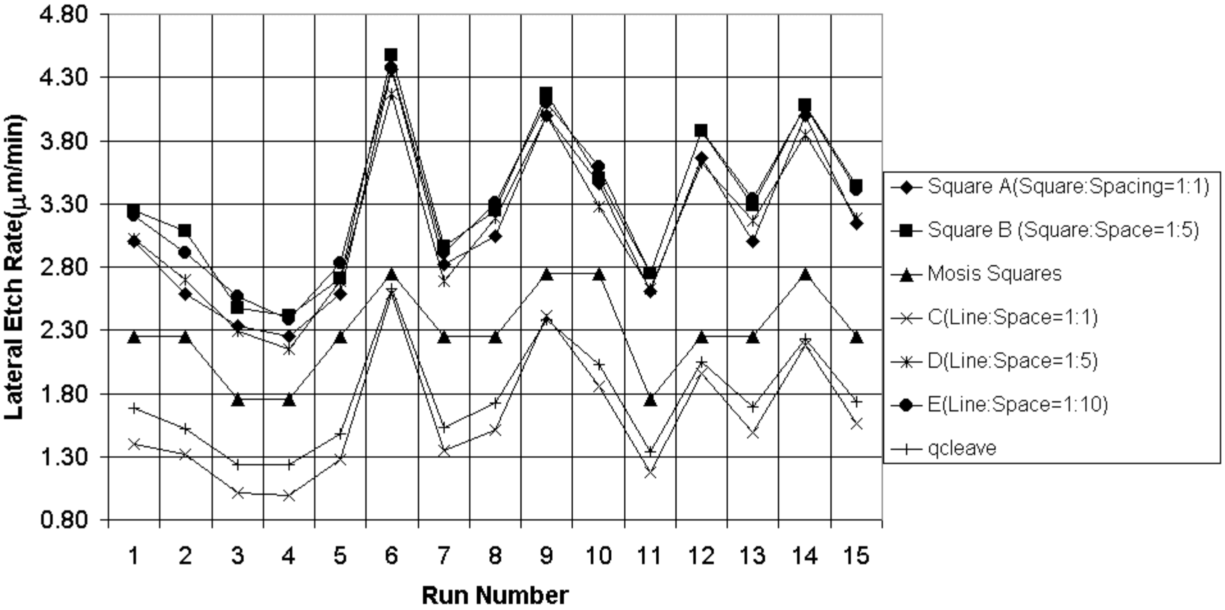


Figure. 3-13. **Lateral etch rate(*m*m/min) of different patterns in statistical experimental runs.**

The etch rates on all patterns follow the same trend.

Square patterns are chosen as the benchmark geometry in future processing tests, since the etch rate can be quantized by visually inspecting the checkerboard. The etch rates on other features can be derived from the benchmark etch rate. Hole etching, which is the key

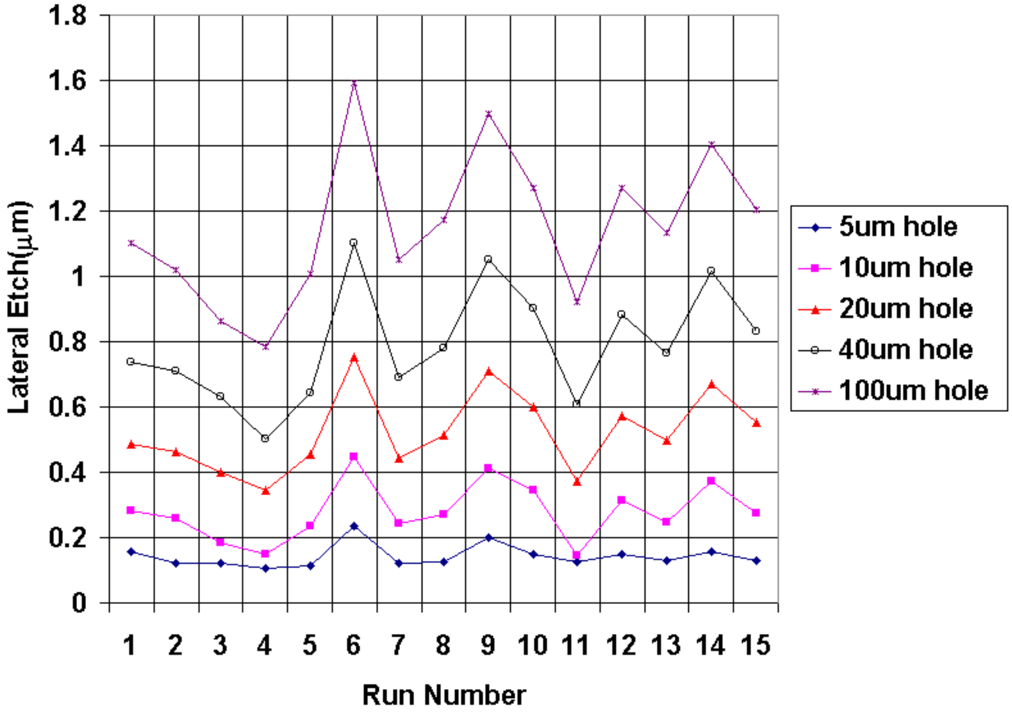


Figure. 3-14. Lateral etch rate (mm/min) on different size of holes (hole width:space=1:5) in statistical experimental runs.

point for release of plates, is much slower compared with that of squares. When the hole opening is small, *e.g.* 5 μm, the etch rate is less sensitive to the system parameter variation. As seen in Figure 3-14, the geometry constraint plays a dominant role.

Response surface results from the design of experiment are given in Figure 3-15. Pressure is the most important factor in determining the lateral etch rate, followed by the SF$_6$ flow rate and the platen power. The etch rate increases with decreasing the chamber pressure and increasing of the SF$_6$ flow; it is not significantly affected by the platen power especially under the high pressure. The relation of the etch rate with the pressure is different from the result obtained from a parallel-plate system. With the high density ion flux in the ICP system, the etching surface is saturated with F$^+$ ions, which is not the case in a

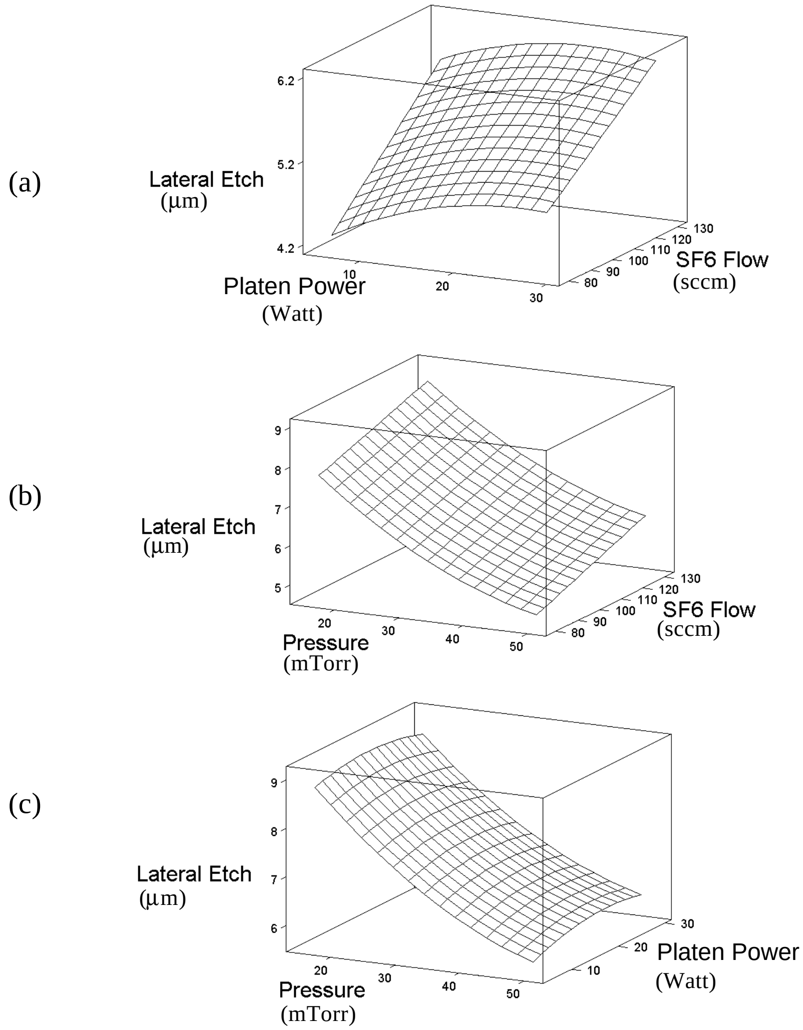


Figure. 3-15. **Response surface on lateral etch of a square checkboard mask with Width: Spacing = 1:5.**
(a) With fixed processing pressure, at 50 mT.
(b) With fixed platen power, at 29 W.
(c) With fixed SF_6 flow rate, at 130 sccm.

parallel-plate system. The ion flux density is primary determined by the coil RF power in the ICP system, instead of the pressure and platen RF power in a parallel-plate system which are less efficient. In the ICP system, how fast gaseous by-products from the reaction can be evacuated from the chamber determines the etch rate. The fastest etch rate in run #6 (16 mTorr processing pressure), 18 W platen and 130 sccm SF_6 flow) is about 45% faster than that of run #2 (50 mTorr processing pressure, 18 W platen and 130 sccm SF_6

flow), which is the screening experiment condition. The etch rate on the whole wafer test is slowed down due to the fact that the exposed silicon area is about 1655 times larger than a single 4 mm^2 dice.

The data generated by the response surface design is again analyzed by Least Square Regression (LSR) analysis software from Minitab® [62] which determines the model coefficients by minimizing the residual variances. The coefficients of Eq. (2.2) in Chapter 2 for benchmark square pattern testing patterns are enumerated in Table 3-3. The quality of the model can be determined by examining the adjusted-R^2 number [55]. A perfect fit would have an adjusted-R^2 value of 100%. The adjusted-R^2 for the etch rate model is 99.3%. This value indicates that the parametric model represents this processing accurately.

Table 3-3: Coefficient of the Full Quadratic Model

Coeff. Term	Coeff. Value	Unit
b_o (Constant)	12.056	μm
b_1 (Pressure)	-3.142	μm/mT
b_2 (Platen Power)	0.392	μm/W
b_3 (SF_6 Flow)	1.104	μm/sccm
b_4 (Pressure^2)	0.847	$\mu m/mT^2$
b_5 (Platen power ^2)	0.014	$\mu m/W^2$
b_6 (SF_6 Flow^2)	-0.036	$\mu m/sccm^2$
b_7 (Pressure * Platen Power)	0.250	μm/(mT*W)
b_8 (Pressure * SF_6 Flow)	-0.367	μm/(mT*sccm)
b_9 (Platen Power * SF_6 Flow)	0.092	μm/(W*sccm)

The etch rate on different patterns in different runs of the factorial design normalized to the width:spacing ratio of 1:5 square checkerboard pattern is in Figure 3-16. The aver-

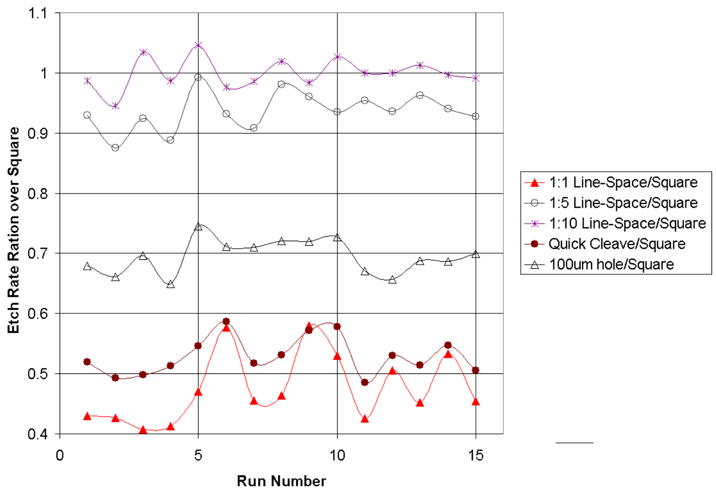
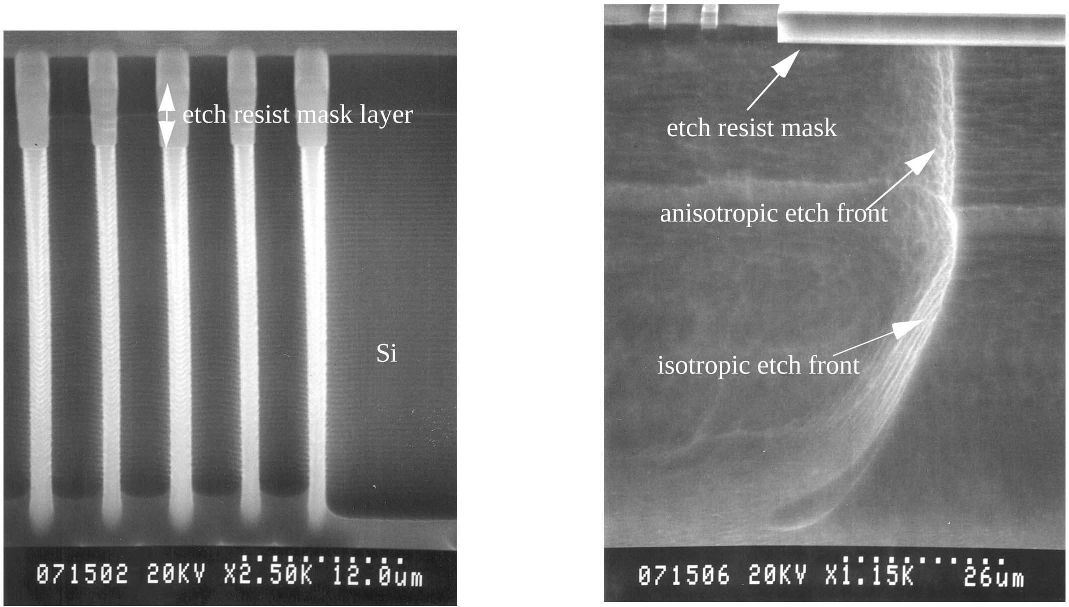


Figure. 3-16. The ratio of etch rate for different patterns normalized to that of the 1:5 square.

age ratio of etch rate of 1:1, 1:5, 1:10 line/space, quick cleave, and 100 µm square holes with hole size:hole spacing = 1:5 to that of square pattern is 0.475, 0.936, 1.000, 0.529 and 0.695 respectively. From the data, it is obvious that long rectangular etch pits with the ratio of the spacing over trench width greater than 5 have similar etch characteristics to squares. This indicates the geometric constraint to the etch is not dominant in this case, and the patterns have similar efficiency of mass transportation in etch reactions. On the other hand, the 100 µm etch holes may be considered as a big opening, but the geometric configuration limits the mass transportation, and slows down the etch rate.

Scanning electron microscopy (SEM) pictures of the etch profiles in Figure 3-17 show the decoupling of the lateral and vertical etch. Undercut of the Ti/W layer is not observed in the processing time window. One demonstration etch is shown in Figure 3-18, where the deep Si etch in the process has been exaggerated. After more than 100 µm deep Si etching, the 2.1 µm wide, 5µm tall microstructures survive, and they suspend a plate


etch resist mask layer
Si
071502 20KV X2.50K 12.0um
etch resist mask
anisotropic etch front
isotropic etch front
071506 20KV X1.15K 26um

(a) (b)

Figure. 3-17. **SEM corresponding to the post-CMOS processing step shown in Figure 3-3 (b) and (c) steps.**
(a) Side-view after silicon deep trench etch.
(b) Side-view after silicon isotropic etch, the final release step. The vertical etch front near the top comes from the vertical anisotropic Si etch and is etched inward by the isotropic Si etch.

about 50 µm above the silicon substrate.

3. 5. 4 Discussion

- **The mass transportation limitation**

A great advantage of the ICP system is the separation of the power generating plasma from the power performing the etch. For the Si isotropic etch, the ICP system has a DC bias much lower than a parallel-plate RIE system. It is expected the etch will be dominated by the chemical mechanism.

From Figure 3-19, it is very clear that the isotropic etch rates of Si strongly depends on the hole size. From all etch recipes, the etch rate has a linear relationship with logarithmic

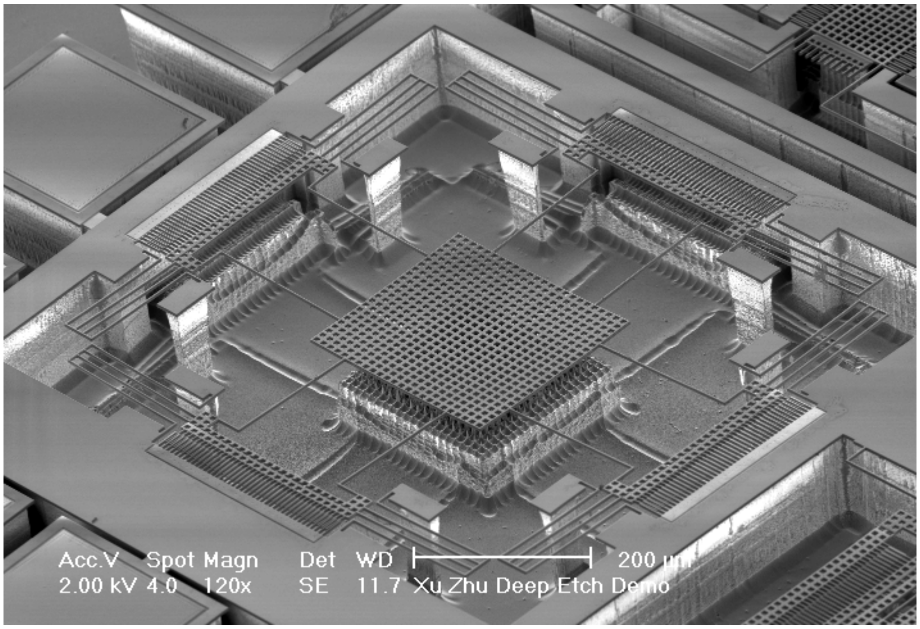

Acc.V Spot Magn Det WD 200 μm
2.00 kV 4.0 120x SE 11.7 Xu Zhu Deep Etch Demo

Figure. 3-18. **Demonstration of deep silicon etch combined with silicon isotropic etch, the mechanical structure is suspended from silicon substrate by about 50 mm (design courtesy of Mike Kranz).**

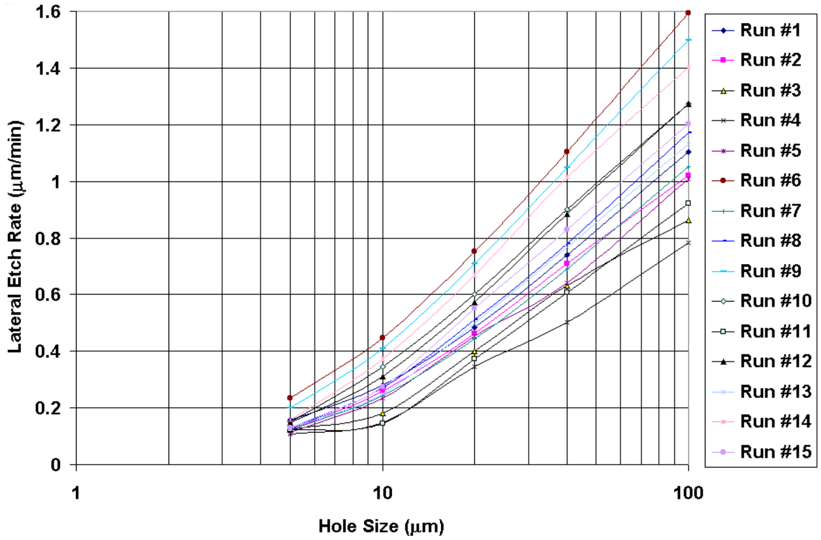


Figure. 3-19. **Lateral etch depth (mm) vs. hole size (hole size:hole spacing = 1:5) on different size of holes in statistical experimental runs.**

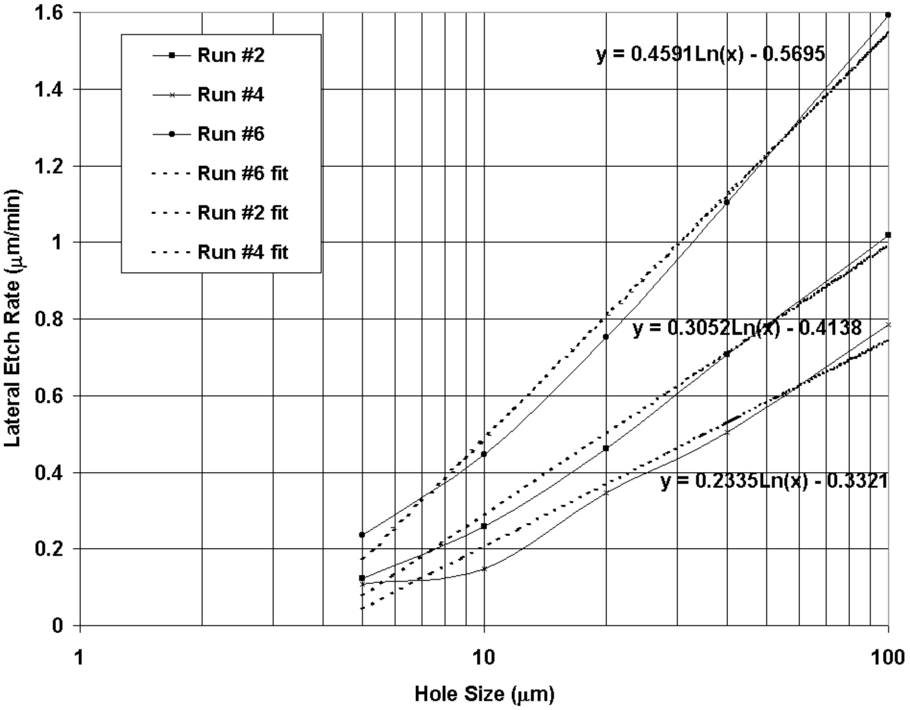


Figure. 3-20. **The relationship of etch rates to the hole sizes under fast, medium and slow etch recipe.**

progression of the hole size, according to the theory of the flow conductance. The fast etch recipe (run #6), the medium speed etch recipe (run #2) and the slow etch recipe (run #4) are modeled in Figure 3-20 as:

$$\text{run \#6: } Y = 0.4591\ln(x) - 0.5695 \quad (3.12)$$

$$\text{run \#2: } Y = 0.3052\ln(x) - 0.4138 \quad (3.13)$$

$$\text{run \#4: } Y = 0.2335\ln(x) - 0.3321 \quad (3.14)$$

where, Y is the etch rate in μm/min, and x is the square hole size in μm. Each regression fitting has the value of R^2 97.3%, 97.1% and 94.7% respectively. In general, the relationship of the etch rate *vs.* hole size can be modeled as:

$$Y = k\ln(x) + c \quad (3.15)$$

where c is constant and k is dependent on process setup. Larger k value indicates a faster etch rate.

3. 6 SUMMARY

In this chapter, both the anisotropic and the isotropic etch of Si by ICP DRIE system have been characterized. The etch lag, which is the most important factor determining the process time, has been well studied. The experimental data show that, in both the vertical and the lateral directions, the etch rate linearly increases with the logarithmic progression increase of the etch pit opening. This observation serves as a guideline in extracting the design rules of the post-CMOS micromachining in the following chapter.

4

Design Rules for Post-CMOS Micromachining

4. 1 INTRODUCTION

As the post-CMOS micromachining technology becomes mature, the concept of using an existing semiconductor foundry to build MEMS devices with minimum add-on steps is increasingly attractive. This technology is leveraged through multi-project wafers as a cost-effective proof-of-concept platform to prototype products and to conduct research. These wafers go through the same process flow described in Figure 3-3. Diverse designs arise for diverse applications, with no pre-defined MEMS layout. Designers expect to receive released (free-standing or free-moving) mechanical structures with no alternation of CMOS specifications. In order to meet all customer expectations, processing information, which quantitatively describes the capabilities and limitations of the process under predetermined processing conditions and parameter settings, is necessary and crucial for the successful MEMS device designs. This information is abstracted as MEMS design rules and is embedded in the verification engine in the design environment. As illustrated in Figure 4-1, the set of design rules functions as a protocol such that MEMS designers work within process constraints and process engineers control the process to satisfy speci-

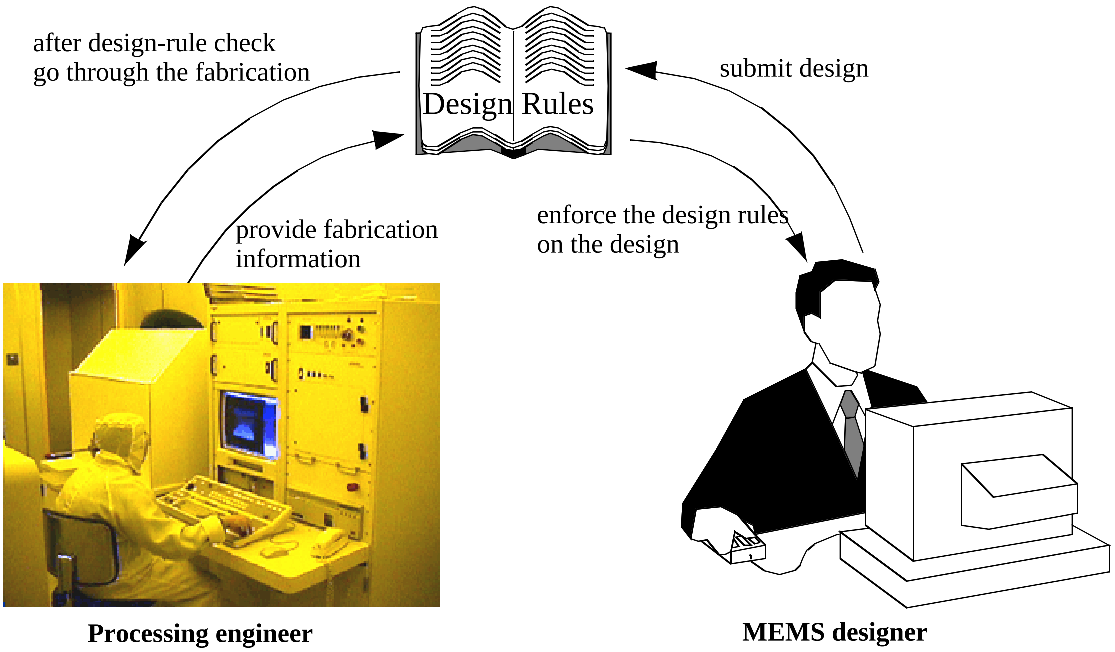

after design-rule check
go through the fabrication
Design Rules
submit design
provide fabrication
information
enforce the design rules
on the design
Processing engineer
MEMS designer

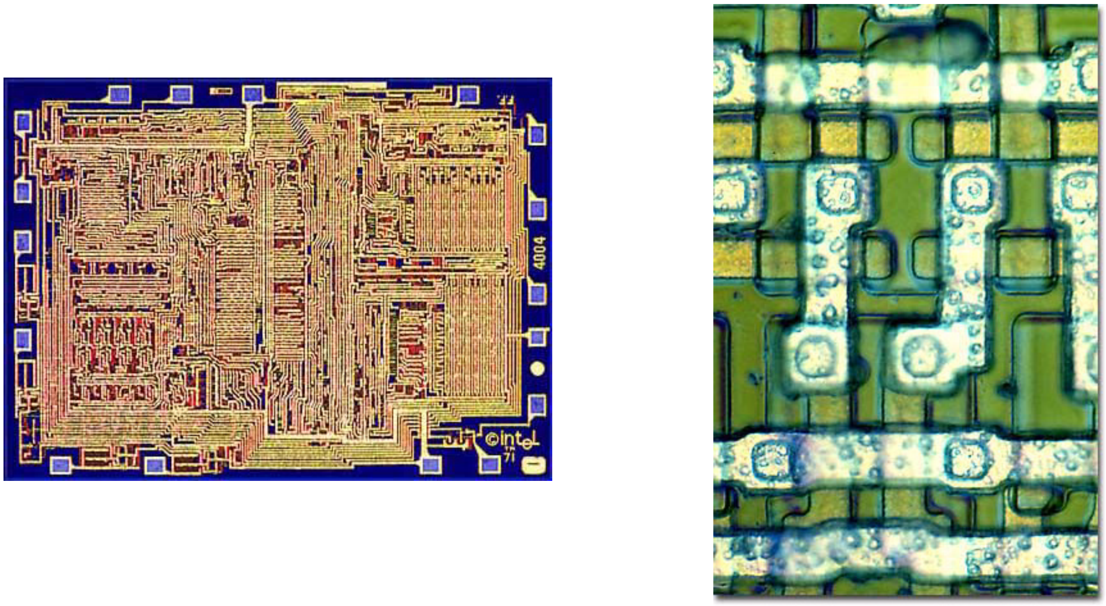
Figure. 4-1. **Design rules function as a protocol between MEMS designers and MEMS fabrication engineers.**

fications in design rules. This chapter covers the methodology and details of how to construct concise and conclusive design rules and how to precisely extract design-rule values from experimental results.

4. 2 THE DESIGN OF TEST STRUCTURES FOR DESIGN RULES

CMOS design rules are well defined by different CMOS foundries, and only the design rules for mechanical structures are discussed in this chapter. These MEMS design rules add further constraints to layouts.

Analogous to application of CMOS design rules, a complicated micromechanical layout is "disassociated" into small pieces, and MEMS design rules contain only fundamental geometries directly related to the post-CMOS micromachining process. There are different ways to break up a layout into basic elements. For example, from the designer’s point of view, a circuit is usually partitioned and analyzed by the function of individual components: devices and interconnects. The devices contain active devices (*e.g.* transistors, diodes) and passive devices (*e.g.* resistors, capacitors and inductors). The interconnects include in-plane wires, pads and vias which connect multiple metal layers. However, as illustrated in Figure 4-2, a dense mesh-like pattern is the processing engineer’s usual view for a full chip. The critical information on the geometric patterns includes the size of each feature, the spacing between features and the overlap of features. These geometric data, required in the design, leads to evolutions of processes and ensures successful fabrication of microelectronic circuitry. A set of geometric constraints, design rules, are then based on the final process. Design rules are expressed in the design-rule file used in layout tools, such as Cadence Virtuoso® or Magic.



(a) (b)

Figure. 4-2. **Optical microscope picture of Intel® 4004 microprocessor.**
(a) Full chip view.
(b) Partial chip view.

This philosophy to encode the CMOS fabrication capability in the form of design rules also applies to the capability of MEMS processes. A post-CMOS micromachined chip can be partitioned into a released area (containing free standing parts and free moving parts) and a non-released area (anchored parts), according to the mechanical behavior after all processing is completed.

The goal of post-CMOS processing is the final result of releasing microstructures and maintaining critical dimensions. There are practical difficulties in monitoring each intermediate process steps, therefore characterization of the process to extract design rules is performed at the end of the entire process flow. In order to overcome etch lags issues discussed in previous chapters, a 15% over etch, based on the measurement in the wide-open etch pit, is used in the dielectric etch step to reach the Si substrate at narrow gaps. Therefore, failure of releasing structures due to leftover SiO_2 blocking the Si etch is minimized.

An overview of a typical post-CMOS MEMS device is shown in Figure 4-3(a). The anchored part is the area outside of the white dash-line box on SEM, whereas the released part is the area inside the white box. The anchor portion is on the top-right corner of the close-up SEM photo, shown in Figure 4-3(b). In order to allow the reactive radicals in the plasma to undercut MEMS structures, sufficient paths for the gas flow are required. These paths can surround mechanical structures, so that the undercut can happen from the periphery of the structures. The gas flow can also pass through structures via etch release holes. Figure 4-4 illustrates various situations for reactive species undercut: from one side of the structures toward the anchor region, from both sides of beam structures, or outward through etch release holes on plates.

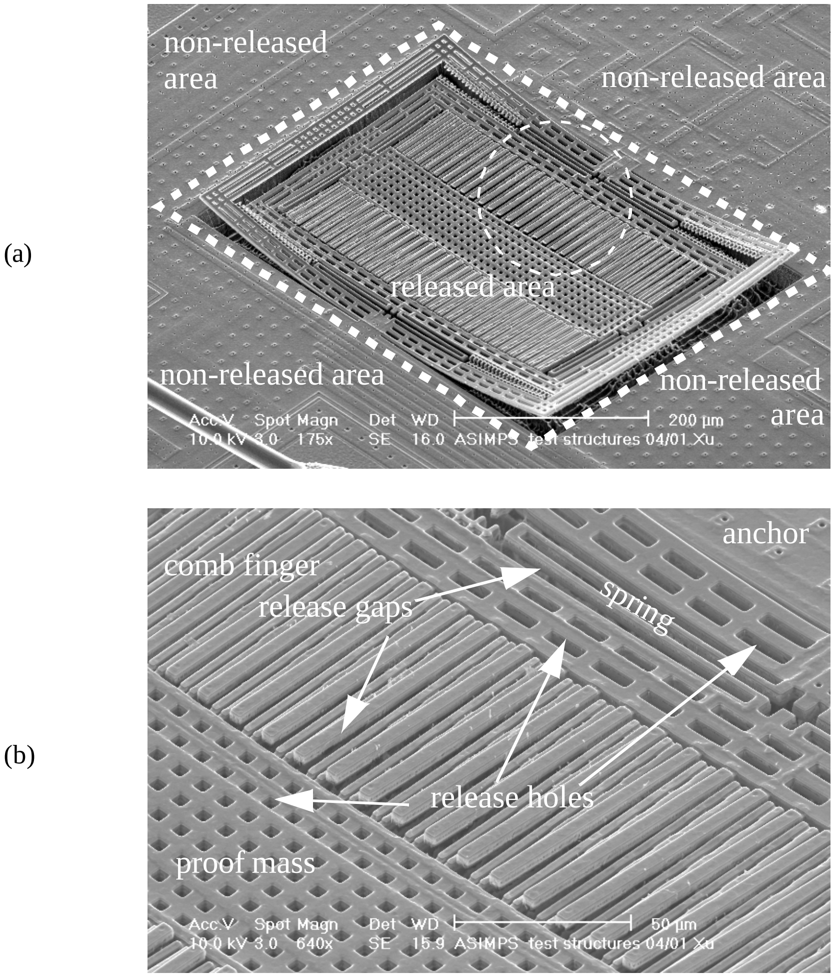

(a)
non-released area
non-released area
released area
non-released area
non-released area
Acc.V Spot Magn Det WD 200 µm
10.0 kV 3.0 175x SE 16.0 ASIMPS test structures 04/01 Xu
(b)
anchor
comb finger
release gaps
spring
release holes
proof mass
Acc.V Spot Magn Det WD 50 µm
10.0 kV 3.0 640x SE 15.9 ASIMPS test structures 04/01 Xu

Figure. 4-3. **Partitioning of a MEMS device for design-rule checking.**
(a) Mechanical structures are divided into a released area inside the white dotten frame and a non-released area, outside the white frame.
(b) A zoom-in SEM photo inside the white circled area illustrates the basic geometric features of beams, gaps, and holes for release.

Theoretically, any shape of the feature which opens a gas flow path from the top of the chip to the substrate is suitable for the purpose of undercut. However, in current microelectronic fabrication, Manhattan layout is preferred, or at least convenient. The majority of CMOS foundries only accept patterns with edges which are parallel, perpendicular or 45° with respect to the horizontal/vertical alignment lines. Historically, mask pattern generators formed mask features by catenating many tiny rectangular patterns. These rectan-

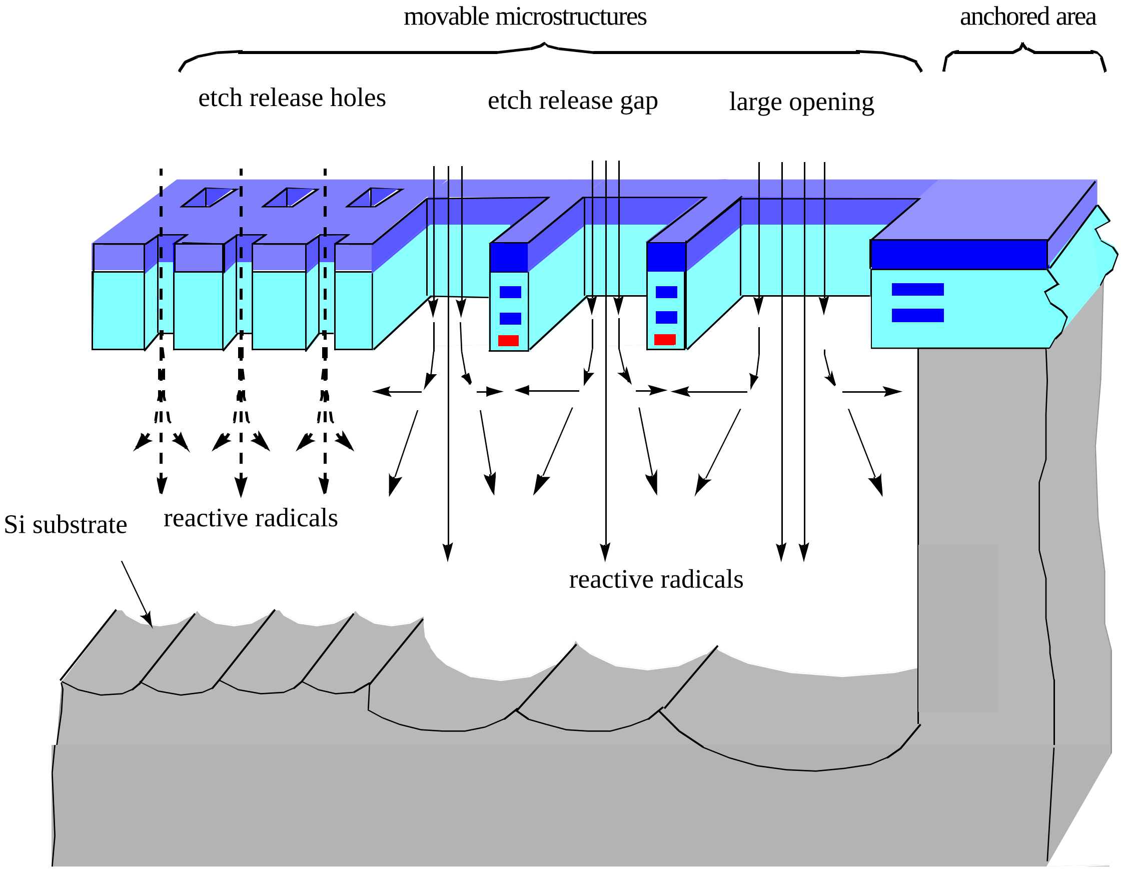

movable microstructures
anchored area
etch release holes
etch release gap
large opening
Si substrate
reactive radicals
reactive radicals

Figure. 4-4. Cross section of typical MEMS structures reveals the undercut of MEMS structure can go from MEMS structure periphery; or the reactive gas goes through the etch release holes and etch outward. Three basic elements need to be implement in MEMS design rules. They are the hole undercut rule, the gap undercut rule and the large opening undercut rule.

gular patterns were achieved by flashing UV lights through adjustable rectangular openings defined by four movable blades. Non-Manhattan features require more and smaller rectangular patterns to approximate the geometry, and therefore, require a larger data base and longer exposure time, which leads to higher cost. Today, raster-scanning mask-making technologies, such as e-beam or laser systems, can overcome the difficulties mentioned above, but non-Manhattan shapes approximated by a smaller raster-beam size still require more time in fabrication. Furthermore, in the CAD verification of layout, there are no good implemented solutions to non-Manhattan layout induced complexity and the time consumption. Therefore, only Manhattan and 45° design verification algorithm are implemented, and only Manhattan rules and 45° rules are specified.

Following the practice of CMOS fabrication, this work only explores rectangular design rules. The major purpose of this work is to ensure the release of moving/free-standing parts, and to guarantee the integration of anchor parts. The rules related to the release by etching are the focus of this work, and are described in detail in this chapter. Other process related rules are listed at the end of this chapter. According to situations described in Figure 4-4, there have been three features encountered in the MEMS structure layout for the purpose of undercut: large openings, gaps and holes. Test structures illustrated in Figure 4-5 are used to extract design rules.

A large opening undercut rule specifies the maximum undercut can be achieved by the process. Any microstructures wider than this value will not be released. This rule also specifies the minimum size requirement of the anchor layout, and the skirt for bonding pads. Bonding pads are usually on the periphery of the chip for easy access during bonding and no crossing of bonding wires on the top the chip. Therefore, at least one side of bonding pads faces large opening and is lateral undercut during the release. The sites that experience forces during wire bonding should avoid these undercut regions, and bonding pads need extra area to compensate this lateral undercut. Moreover, this large opening rule specifies the minimum space required from the edge of the etch pit to preserve Si area containing circuitry during micromachining. One way to obtain this data is to use SEM to measure the undercut from the periphery of the chip, as illustrated in Figure 3-17(b).

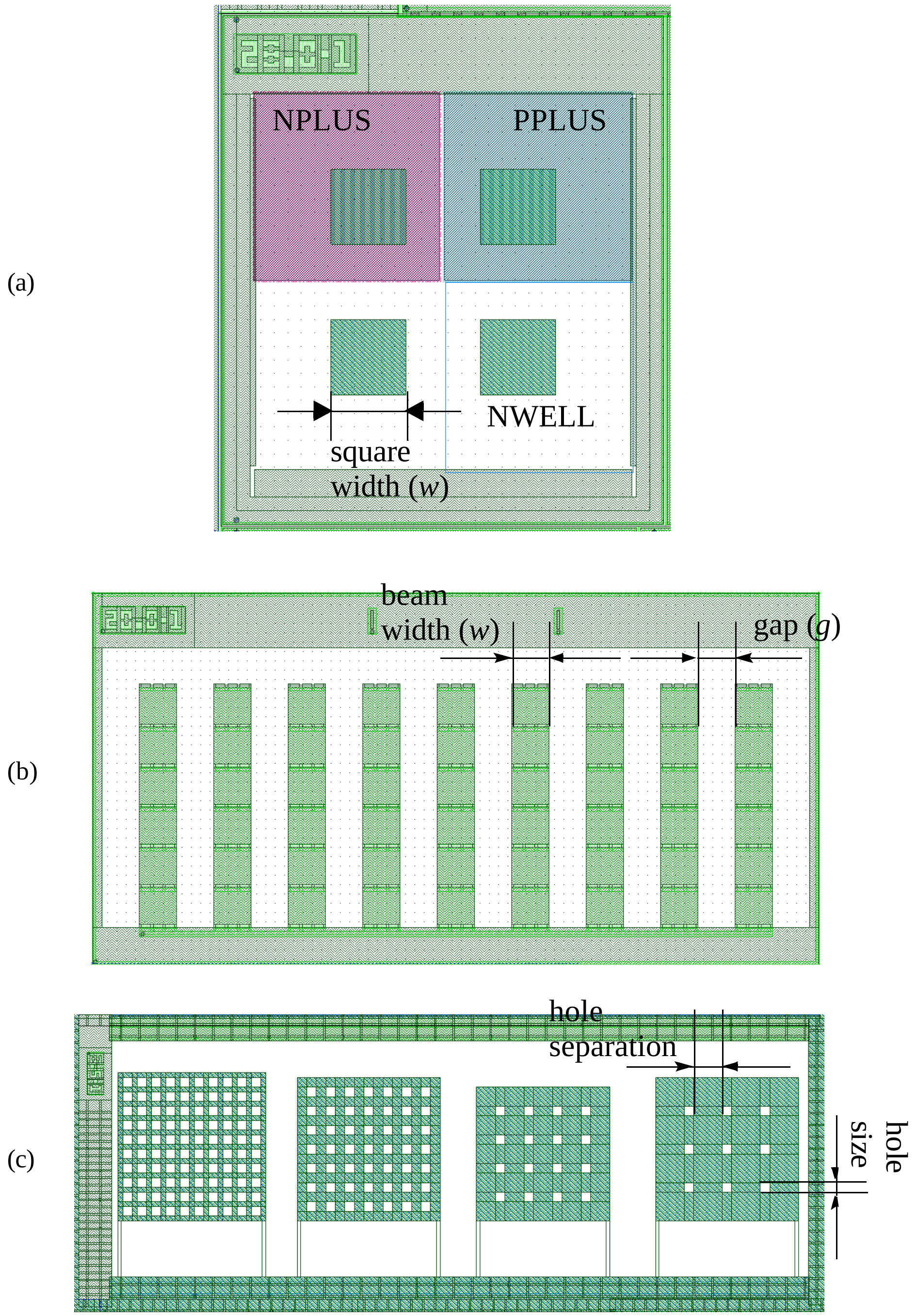

(a)
NPLUS
PPLUS
NWELL
square
width (*w*)
(b)
beam
width (*w*)
gap (*g*)
(c)
hole
separation
hole
size

Figure. 4-5. Layout of three test structures used for extracting MEMS design rules for post-CMOS micromachining.
(a) The square structure - the large opening undercut rule.
(b) The cantilever structure - the gap undercut rule.
(c) The plate structure - the hole undercut rule.

Another way is to use a optical microscope to check which size of square pattern has been released, as in Figure 4-5(a). The undercut value is half the size of square width.

A gap undercut rule is required for releasing MEMS structures such as a comb finger or a spring, as marked in Figure 4-3. The test structure for this rule is a set of cantilevers with the undercut mainly determined from the sides of the beams. To emulate the situation in real layout, such as comb fingers in Figure 4-3, multiple cantilever beams, with equal space between them, are used, as in Figure 4-5 (b). The beam width (w) represents the width of the structure to be released. The gap (g) represents the separation between the structures. The beam should be long enough that the undercut from the tip of the cantilever doesn’t dominate the etch. Since the residual stress induces out-of-plane curling upon release, the release can be easily detected by a white-light-interferometric measurement.

A hole undercut rule is required to release plate structures, such as the proof mass in Figure 4-3. The test structure for this design rule is a set of plates with release holes. These plates are anchored by two thin beams, as in Figure 4-5 (c). Such plates should be large enough to ensure that the release of the plate is determined by the etch release holes and not from the periphery of the plate. Similar to the cantilever test structures, the curling after the release of plates can be detected by the white-light-interferometric measurement.

Extra processing time requires layouts to be modified such that the circuitry is far away from the edge of the mask, all the anchors are wide enough, and all bond pads/probe pads have enough margins for bonding and probing.

For the square test structure, as in Figure 4-5 (a), the etch on different surface doping has been tested. They are *p*-type substrate, *n*-type well on *p*-type substrate, n^+ (heavily-doped *n*-type contact) and p^+ (heavily-doped *p*-type contact) on *p*-type substrate. The spacings between the squares and the spacings from a square to the surrounding anchor mask area are the size of the square. This is to ensure that squares are uniformly etched from all directions.

For each group of cantilever test structures, as in Figure 4-5 (b), the widths of all cantilever beams are the same value. The spacings between beams and from tips of cantilever beams to anchor mask areas are the same value. The beams are 120 μm long, which are much longer than undercuts.

For each group of plate test structures, as in Figure 4-5 (c), the size of release holes is the same value on all the plates. The separation between holes is the same value on the same plate but varies between plates. The length of anchor beams is 50 μm. The spacing from the plate to the anchor mask area is 5 to 20 μm, and the spacing between each plate is 30 to 40 μm. The size of the plate is a multiple of the sum of the size of the release hole and the separation between the holes, with a rough target of 100 μm wide for the hole size greater than 5 μm and of 50 μm for the hole size less than 5μm. The plates are placed from the left to the right by the same step size, as in Figure 4-5(c). This yields the same footprint of layout with different holes sizes and hole spacings, therefore reduces the burden in assembling different plate test structures into the chip. However, the difference in the plate size with the fixed footprint size yields different separation between plates and between the plates and the anchor frame.

4. 3 MEASUREMENT RESULTS AND EXTRACTED DESIGN RULES

As mentioned above, the undercut of squares is obtained by optical microscope inspection. This technique requires that the square be large enough to cover the processing range and that the size increment of the squares be small enough to give the accurate etch data. This step size is 0.2 μm for the experiment reported here. The etch results of cantilever test structures and the plate with release holes are difficult to be measured under an optical microscope. One reason is undercut of the anchor region used as the reference, and the reference curls up as with cantilever beams. A Veeco/Wyko NT3300 white-light-interferometric microscope provides an easy way to determine release as released structures curl out of the plane. Typical images comparing released structures *vs.* unreleased structures are shown in Figure 4-6.

The measurement results on the test structures are shown in the Figure 4-7, Figure 4-8, and Figure 4-9. The isotropic Si etch time provides a trade off between maximum allowable structural width and minimum spacing of electronics from etch pits. For each type of feature, the data based on 3 min, 5 min and 7 min isotropic Si etch (130 sccm SF6, 50 mTorr, 600 W coil power and 12 W platen power) are given. The 5 min data is used for the standard process to derive post-CMOS micromachining design rules. The 3 min etch and the 7 min data are used to specify the upper and lower boundary of the reasonable process window suitable for post-CMOS micromachining. Figure 4-7 summarizes release results for the beam width *vs.* the release gap, which lead to gap undercut rules. Figure 4-8 shows experimental results of release holes in the plate structure, which correspond to hole undercut rules. In both Figure 4-7 and Figure 4-8, the Y-axis are half of the beam

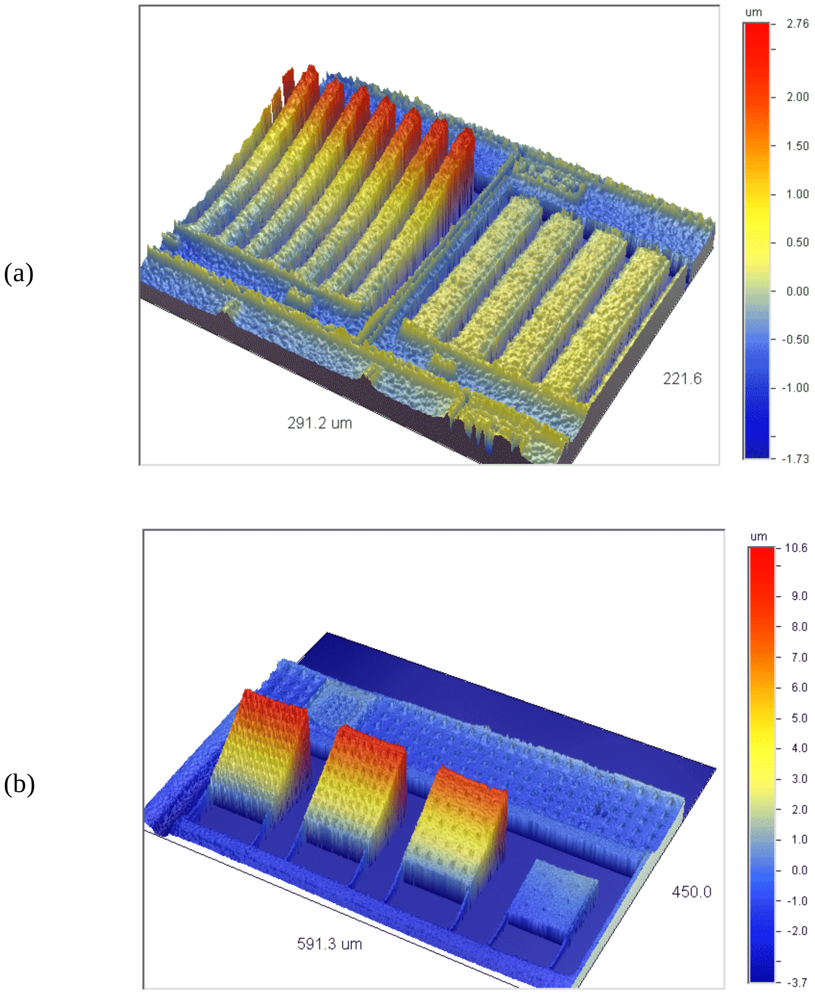


Figure. 4-6. **3-D images on results of released vs. un-released test structures.**
(a) Beam-gap test structures, the beam on the left side are released and the four beams on the right side are still anchored to substrate.
(b) Test structures of etch release holes on the plates. Three plates on the left are released and the one on the right is still anchored to substrate.

width instead of the beam width in physical layout. In this way, the data in Figure 4-7 and Figure 4-8 specifies the lateral undercut in these two typical etch pit pattern instead of the undercut for the two specific types of microstructures. Therefore, these measurement results can be integrated into the design rules check engine discussed in the later chapter. In both Figure 4-7 and Figure 4-8, the grey-solid dots represent the measured data with structures released, and the open dots indicate the measured data with structures not released. A solid line links the data which is marked with a cross and is the estimated boundary between the unreleased structures and released structures. This projected line is based on the knowledge of processing characterization data obtained from the previous processing characterization chapters. However, this line is not the actual boundary separating released structures and unreleased structures for three primary reasons. First, layouts of test structures on the fabricated chips do not cover the entire range adequately and sometimes lack desired spatial resolution. This is very obvious in the Figure 4-7 and Figure 4-8(a). Second, the photolithography variation and misalignment of stack metal layers induce deviation of the MEMS structure dimensions of around 0.3 μm. Third, polymer generation during the dielectric etch, discussed in the next chapter, contributes to the variation of measurement data by changing the size of etch pits. In Figure 4-8(c), small plates were released by the undercut from large openings around plate edges. Therefore, no useful information can be gathered. The second-generation structures, shown in the last section in this chapter, will eliminate this problem.

The projected line in Figure 4-7 and Figure 4-8 shows that the undercut design regions are divided into an etch-lag-limited zone and an etch-time-limited zone. The undercut in the first zone is limited by the etch-lag effect due to the relatively small size of holes and gaps. Here, the undercut increases with the gap or hole size. The undercut in the second zone is limited by the total processing time. In this zone, the undercut is constant regardless of the increase in the gap or hole size. The large opening undercut is dominated by the etch-time-limited effect. The values obtained from the large opening undercut is the maxi-

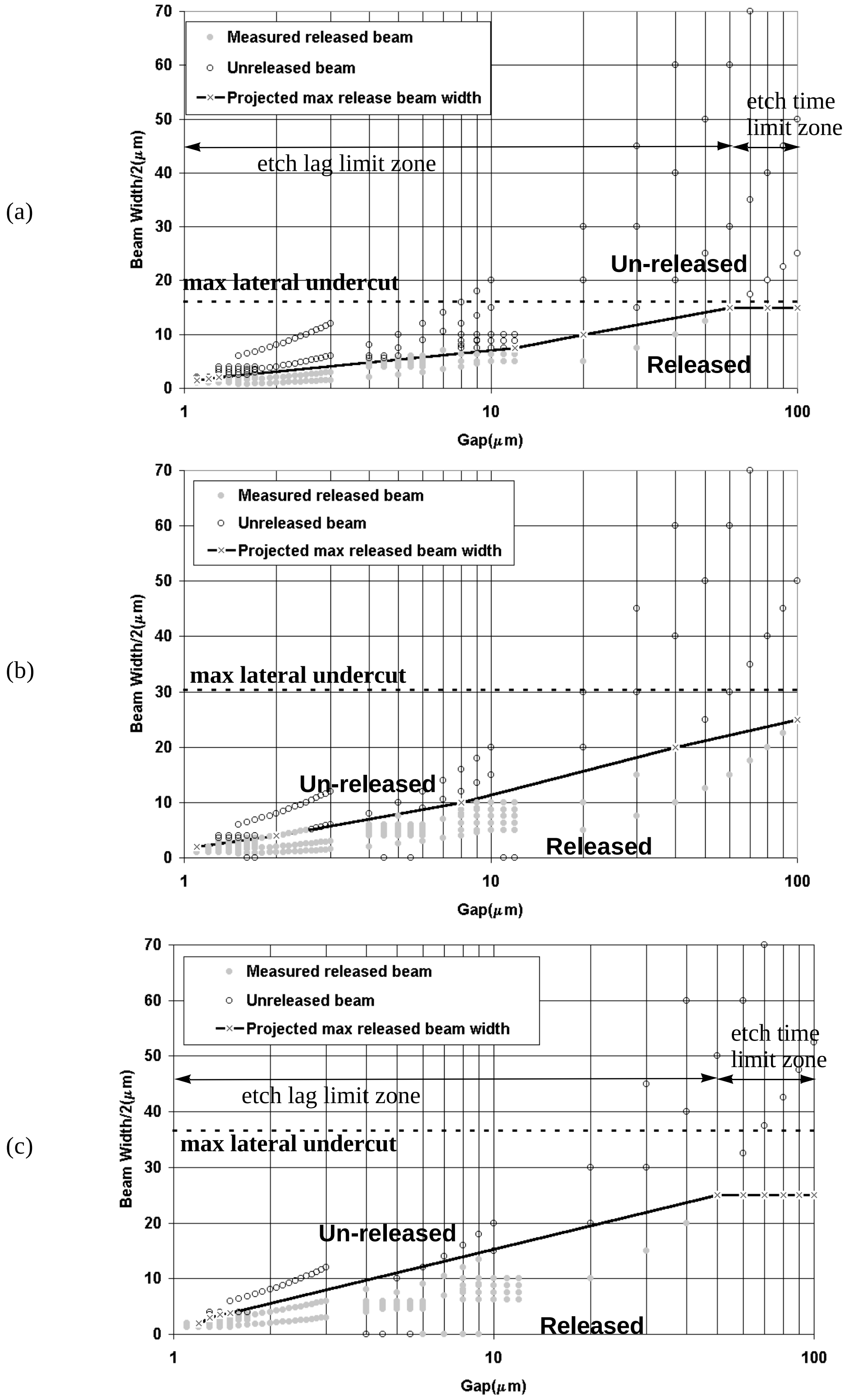


Figure. 4-7. Summary of design rules for the trench space (beam width) vs. trench width (gap) for 3 min (a), 5 min (b) and 7 min (c) isotropic Si etch.

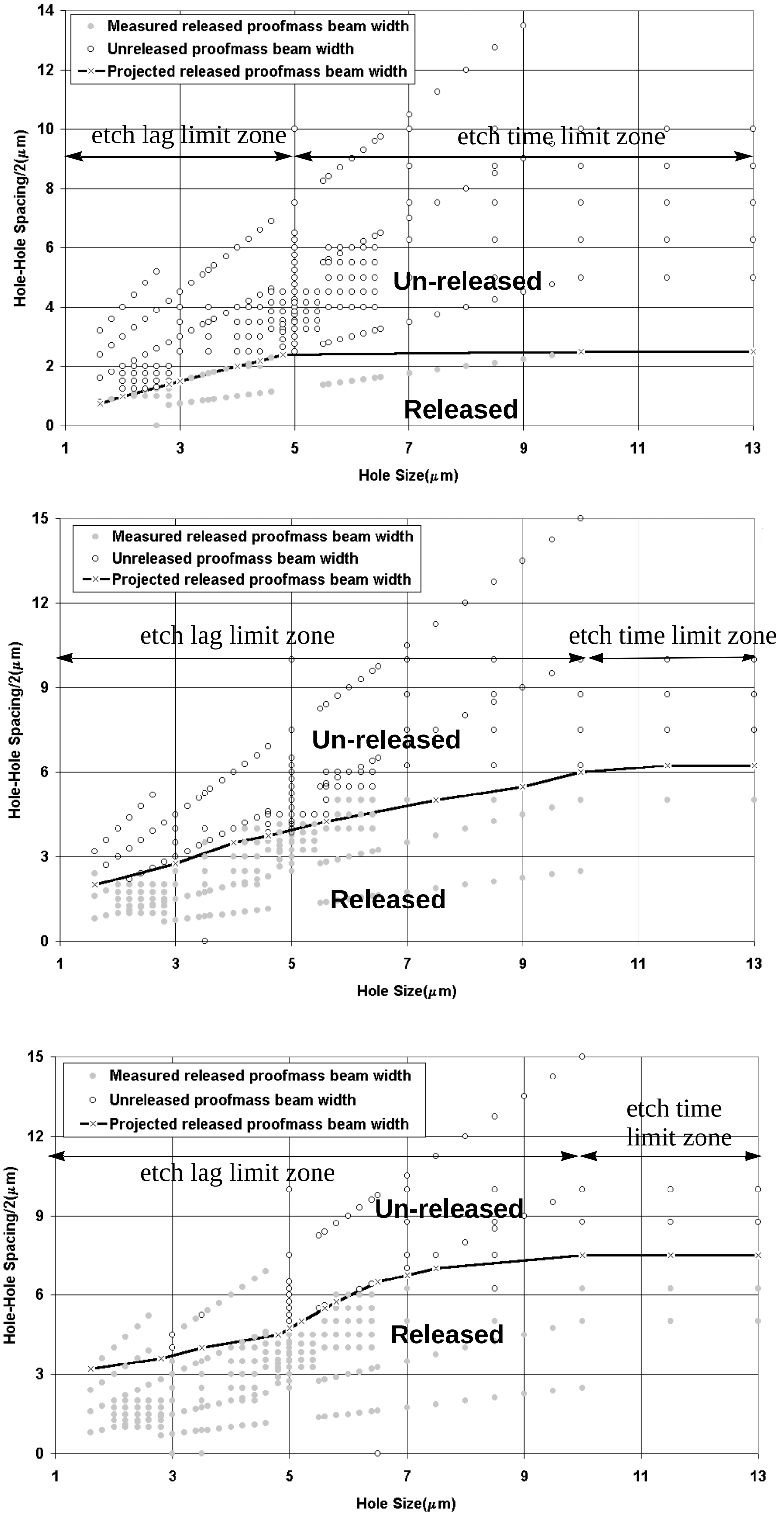


Figure. 4-8. **Summary of design rules for the structures with etch release holes on the plate: etch release hole separation (beam width) vs. release hole size for 3 min (a), 5 min (b) and 7 min (c) isotropic Si etch.**

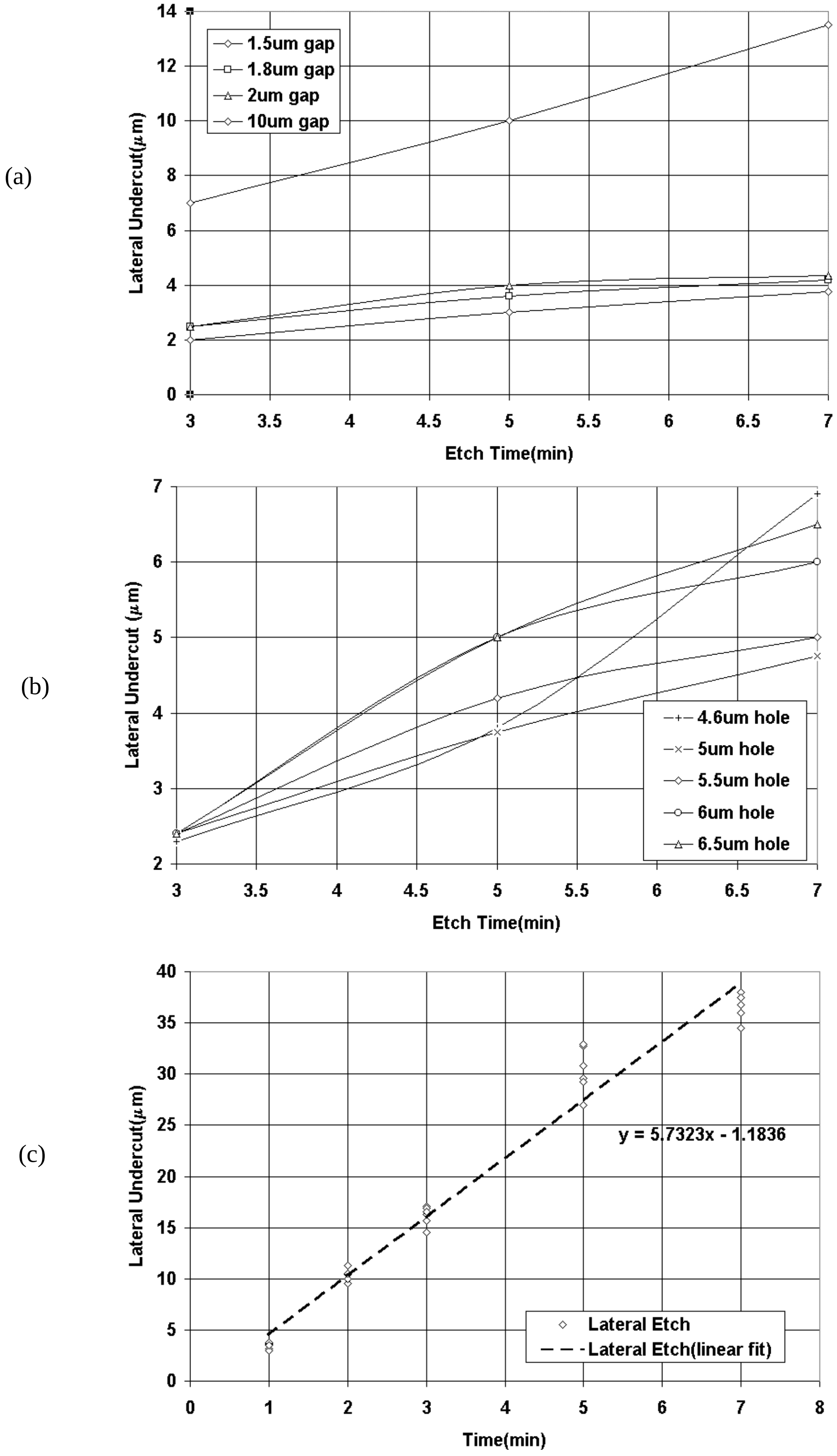


Figure. 4-9. **Summary of lateral etch depth vs. etch time on MEMS design rule different test structures, (a) cantilever, (b) plate, and (c)large open etch pit (square).**

mum achievable undercut in the etch. The values are marked as a horizontal line in Figure 4-7 and Figure 4-8.

The Figure 4-9 shows the lateral undercut *vs*. etch time for the three test structures identified in this chapter. The lateral undercut changes linearly with the etch time. Figure 4-9(c) shows the lateral undercut *vs.* the etch time for a big opening etch pit, which can be obtained approximately by using square test structures or can be obtained accurately by measuring the lateral etch depth of an anchor structure surrounded by large open etch pit, which is adopted here. The data shown in Figure 4-9 are collected on the Surface Technology Systems (STS) etcher installed in the Carnegie Mellon University facility, whereas, and the data shown in Figure 3-10 are collected on the STS tool installed in the Cronos Inc. facility. Although the same processing parameters are used in both etching tools, there is about 20% difference in the etch rate. The system at Carnegie Mellon University has a new generation of RF power source and a new generation of vacuum system, therefore the system is more efficient in etching. Figure 4-9(c) shows the maximum Si isotropic etch rate that can be achieved with the selected processing parameters. The size of any MEMS mechanical structure to be released in any design cannot exceed this limitation. The measurement data indicates no significant difference in the etch on different substrate types and substrate doping levels. Therefore, it is sufficient to use one square test pattern instead of four as in Figure 4-5 (a).

As illustrated in Figure 4-9(c), to simplify the plots above, rules of thumb for the MEMS layout with 5 min isotropic Si etch are:

- the hole undercut rule,

$$\begin{cases} Y = 0.462x + 1.49 & 0 < x < 10.33 \\ Y = 6.25 & 10.33 \le x \le 13 \end{cases} \quad (4.1)$$

where Y (in µm) is separation of holes, and x (in µm) is the hole size.

- the gap undercut rule,

$$Y = 5.20\ln(x) + 0.59 \qquad 0 < x \le 100 \quad (4.2)$$

where Y (in µm) is the separation between gaps, and x (in µm) is the size of gap.

- the large opening undercut rule,

$$Y = 30 \quad (4.3)$$

where Y (in µm) is the maximum lateral undercut of Si substrate.

It is noticed that due to the variation in the measurements and the lack of resolution in the design, with 0 min etch, the lateral etch depth is not zero. The second-generation test structures layout all the test structures with values around the first-generation estimated design rules, therefore, more accurate results are expected.

The design rules for 5 min isotropic etch can also be tabulated as Table 4-1 and Table 4-2, because Eq. (4.1) and Eq. (4.2) cannot be directly represented into the DIVA rule file in the Cadence, and step-function approximations are used currently. The large opening undercut rule is 30 µm for the 5 min isotropic etch. In order to compensate for the processing variation, a 10% back off from the design-rule values in Table 4-1 and Table 4-2 is recommended.

Table 4-1: Hole Undercut Rules

hole size (μm)	hole separation (μm)
2.0	4.8
2.4	5.2
3.0	5.8
4.0	6.7
5.0	7.6
5.2	7.8
6.0	8.5
10.0	12.2

Table 4-2: Gap Undercut Rules

gap size (μm)	gap separation (μm)
1.2	3.1
1.5	5.4
2.0	8.4
5.0	17.9
≥ 10.0	25.1

4. 4 IMPLEMENTATION OF DESIGN RULES IN CADENCE DIVA ENGINE

The design rules summarized in Table 4-1, Table 4-2 and Eq. (4.3) have been implemented in the Cadence DIVA Engine in the research work at Carnegie Mellon University. An example of DIVA code to detect the undercut of structure by the gap between structures is shown below. This MEMS design-rule check consists of five steps.

- Step 1: detect the size of gap. The code sorts structures into five pre-determined grade gap sizes, each of which is defined as greater than a predetermined value and it is listed as GAP_XXL, TMP1, TMP2, TMP3 and TMP4:

```
; GAP_XXL: gap width >= 10 μm[1]
```

---

[1] the line begins with “;” are comments in the program.

```
; TMP1: gap width >= 5 µm
; TMP2: gap width >= 2 µm
; TMP3: gap width >= 1.5 µm
; TMP4: gap width >= 1.2 µm
     (GAP_XXL = geomSize[1](geomSize(GAPS -4.999) 4.999))
     (TMP1 = geomSize(geomSize(GAPS -2.499) 2.499))
     (TMP2 = geomSize(geomSize(GAPS -0.999) 0.999))
     (TMP3 = geomSize(geomSize(GAPS -0.749) 0.749))
     (TMP4 = geomSize(geomSize(GAPS -0.599) 0.599))
```

- Step 2: convert the pre-determined gap size into five different categories: XXL size gap (between 10 and 20 µm), XL size gap (between 5 and 10 µm), L size gap (between 2 and 5 µm), M size gap (between 1.5 and 2 µm) and S size gap (between 1.2 and 1.5 µm).

```
; GAP_XXL: 10um<=width<20 µm
; GAP_XL: 5um<=width<10 µm
; GAP_L: 2um<=width<5 µm
; GAP_M: 1.5um<=width<2 µm
; GAP_S: 1.2um<=width<1.5 µm
     (GAP_XL = (geomAndNot TMP1 GAP_XXL))
     (GAP_L = (geomAndNot TMP2 TMP1))
     (GAP_M = (geomAndNot TMP3 TMP2))
     (GAP_S = (geomAndNot TMP4 TMP3))
```

- Step 3: bloat the gap, according to discrete values in design rules, to identify the undercut area.

```
; GAP_XXL_RELEASE: bloat GAP_XXL by 12.55 µm
; GAP_XL_RELEASE: bloat GAP_XL by 8.95 µm
; GAP_L_RELEASE: bloat GAP_L by 4.2 µm
; GAP_M_RELEASE: bloat up GAP_M by 2.7 µm
; GAP_S_RELEASE: bloat up GAP_S by 1.55 µm
     (GAP_XXL_RELEASE = geomSize(GAP_XXL 12.55))
     (GAP_XL_RELEASE = geomSize(GAP_XL 8.95))
     (GAP_L_RELEASE = geomSize(GAP_L 4.2))
     (GAP_M_RELEASE = geomSize(GAP_M 2.7))
     (GAP_S_RELEASE = geomSize(GAP_S 1.55))
```

- Step 4: determine the either released area by merging the results from the five different MEMS DIVA rules.

---

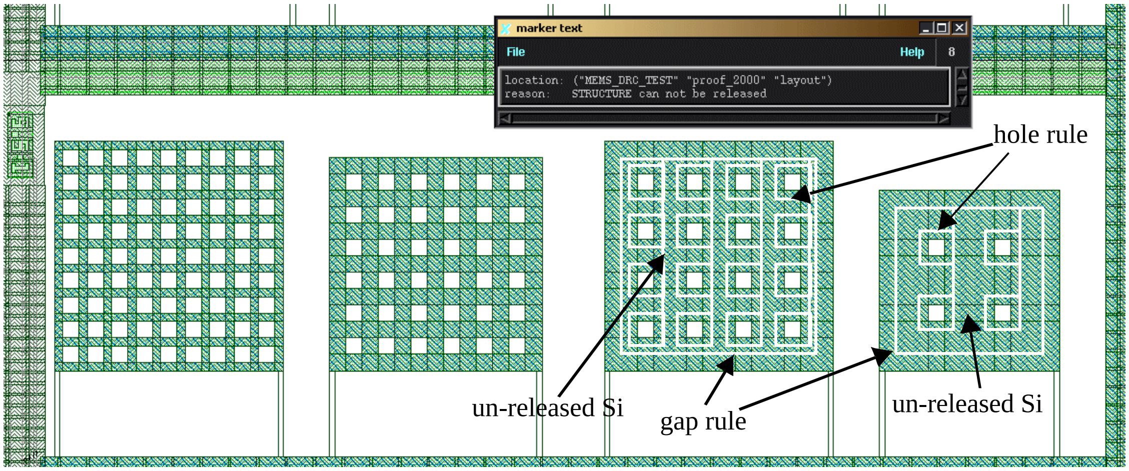
[1] geomSize(feature, value) is a Cadence DIVA command, and it expands the "feature" by the specified "value". If the "value" is positive, the layout "feature" expands from all edges by the specified "value". If the "value" is negative, the layout "feature" shrinks from all edges by the specified "value".

```
(RELEASE = geomOr(GAP_XXL_RELEASE
        geomOr(GAP_XL_RELEASE
        geomOr(GAP_L_RELEASE
        geomOr(GAP_M_RELEASE
        geomOr(GAP_S_RELEASE
        geomOr(HOLE_XL_RELEASE
        geomOr(HOLE_L_RELEASE
        geomOr(HOLE_M_RELEASE
             HOLE_S_RELEASE))))))))
```

- Step 5: determine the unreleased area and mark the unreleased area on the layout.

```
 (UNRELEASE = geomAndNot(STRUCTURE RELEASE))
 (drc UNRELEASE
       (area > 0.0) "STRUCTURE can not be released"
)
```

A demonstration of design-rule check results on one of the hole test structures is shown in Figure 4-10. The white lines indicate the depth of lateral undercut according to the encoded design-rule value. The areas between the white lines are the Si underneath the structure which cannot be removed.



```
location: ("MEMS_DRC_TEST" "proof_2000" "layout")
reason:   STRUCTURE can not be released
```

Figure. 4-10. **The results for one the hole test structures. The while lines, which blinking in the Cadence Virtuoso window, indicates the structure cannot be released according to encoded design rules.**

4. 5 MISC. ITEMS IN MEMS DESIGN RULES

Besides undercut rules, there are some additional details to be taken care of in the CMOS MEMS design [76]. There are two major additions to the aforementioned design rules:

- The polysilicon enclosure rule, as in Figure 4-11, specifies the minimum distance of polysilicon from a structural sidewall defined by a metal layer. This design rule is required because of the misalignment of layers in the CMOS process, the ion-milling effect induced shrinking of the top mask, and retrograde dielectric sidewall profiles after the post-CMOS process. Any polysilicon structure embedded in the MEMS structure must be enclosed by the top mask layer, and a 0.6 µm enclosure is adopted in this work. If the design rule is violated, the polysilicon may be exposed to the plasma during the isotropic Si etch, as in Figure 4-11 (c).
- The metal-overlap rule specifies the minimum metal-to-metal overlap required to guarantee the structural continuity. Due to routing or other design reasons, it is

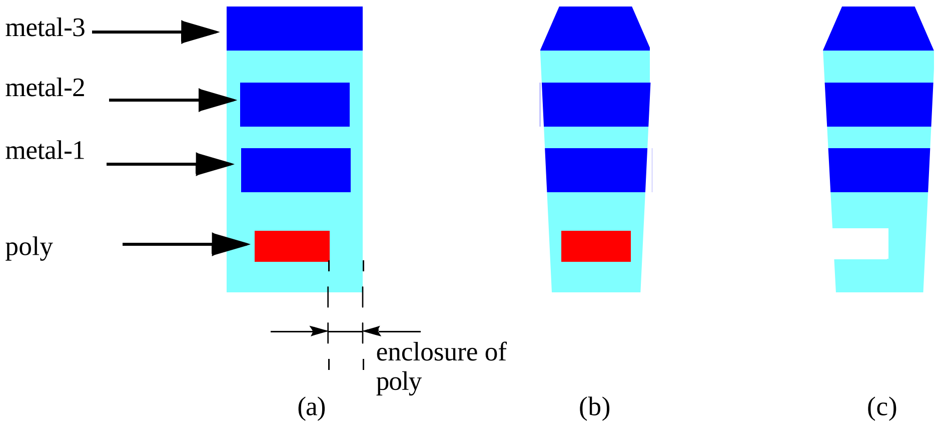


Figure. 4-11. **Illustration of the necessity of polysilicon enclosure rule.**
(a)Cross-section of ideal beam after the process.
(b)Cross-section showing reduced beam width due to ion-milling effect.
(c) Cross-section showing the poly being etched out after Si etch process due to the mis-alignment of the layers.

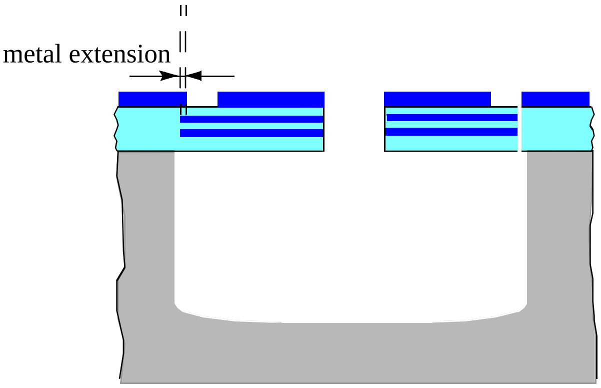


Figure. 4-12. **Illustration of the metal overlap rule. The left side shows a cantilever with the metal overlap, where the extrude part of the structure is still anchored on the substrate. The right side shows a cantilever without the metal overlap, where the misalignment of metal layers creates a gap in the structure, and the structure is etched into two pieces.**

very common to switch the top structural mask to different metal layers. At the metal layer transition area, the overlap of the different metal layers is required. A minimum metal overlap of 0.3 μm is adopted in this work. Without an overlap, the misalignment of different metal layers during fabrication may cause a small gap in the microstructure, as in Figure 4-12 and the released structure may fracture or be simply etched into two pieces.

The release of post-CMOS MEMS structures doesn’t mean the Si is totally removed under the microstructure. Just below the border of released and unreleased structures, a small part of Si may be left on the backside of the microstructure, as illustrated in Figure 4-13. This uncontrolled leftover affects the mechanical properties of the structure. Although this Si helps to reduce the structure curling and lateral bending, it is not recommended to have this uncontrolled Si residue on the back of the structures because of the subsequent wider variation in design properties.

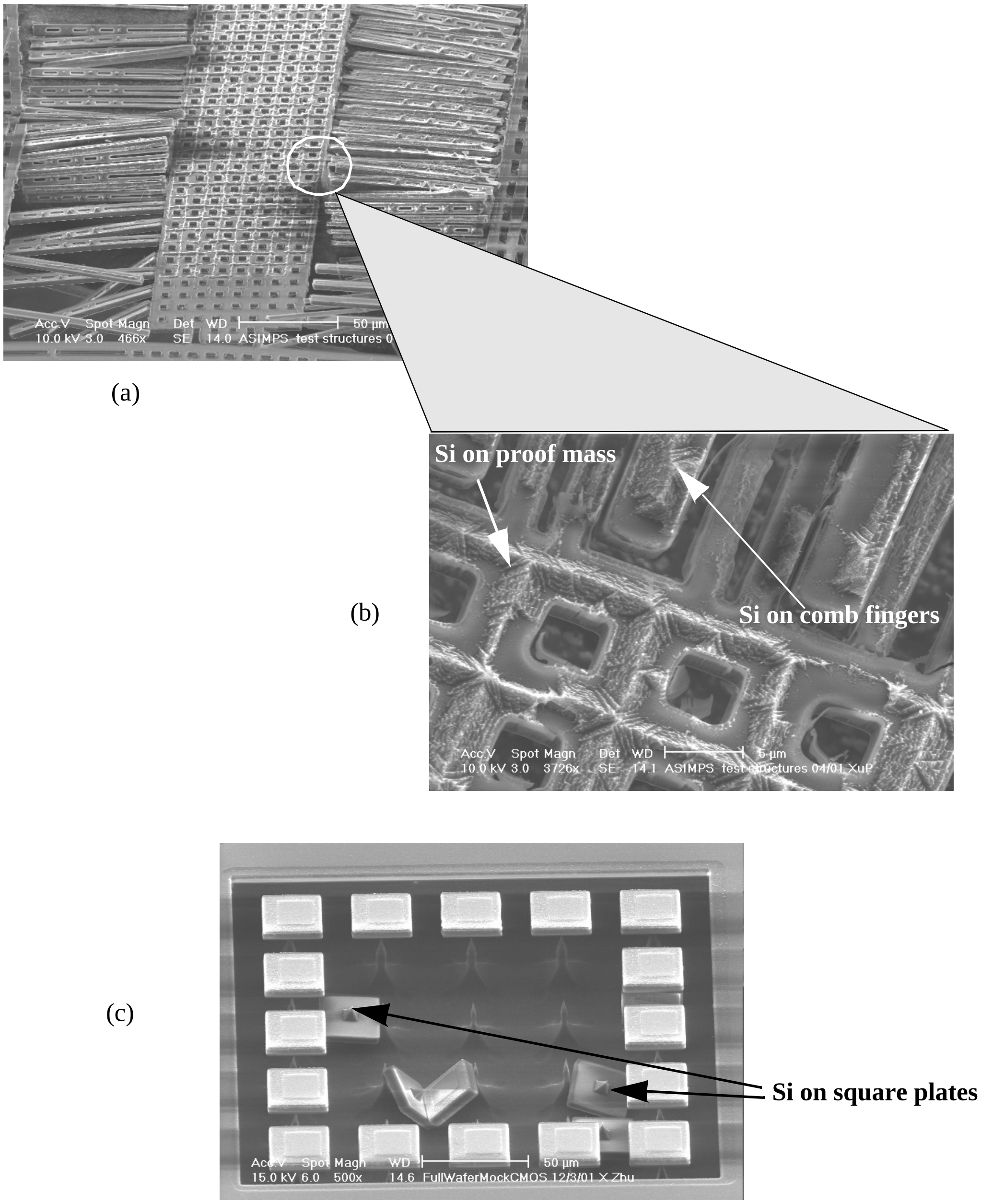

Acc.V Spot Magn Det WD 50 µm
10.0 kV 3.0 466x SE 14.0 ASIMPS test structures 0
(a)
Si on proof mass
Si on comb fingers
(b)
Acc.V Spot Magn Det WD 5 µm
10.0 kV 3.0 3726x SE 14.1 ASIMPS test structures 04/01 XuP
(c)
Si on square plates
Acc.V Spot Magn WD 50 µm
15.0 kV 6.0 500x 14.6 FullWaferMockCMOS 12/3/01 X Zhu

Figure. 4-13. **Evidence of Si left on the back of post-CMOS MEMS structures.**
(a) SEM of a resonator structure, flipped to show the backside.
(b) Magnified SEM shows the Si leftover on the proof mass and comb fingers.
(c) SEM of square pattern test structures with part of squares are released and fall down. The others are still attached to the substrate on the sharp Si tips.

There are two important design observations useful for the design. First, removing the field oxide under the structural layers dramatically reduces the curling, because the field oxide is grown with highest temperature in the CMOS process flow. This can be done in the layout by putting an active layer under structures. This effect is very significant in the processes where the inter-metal dielectric is deposited by spin-on glass, because spin-on glass has a lower processing temperature, which is in contrast to the high stress field oxide

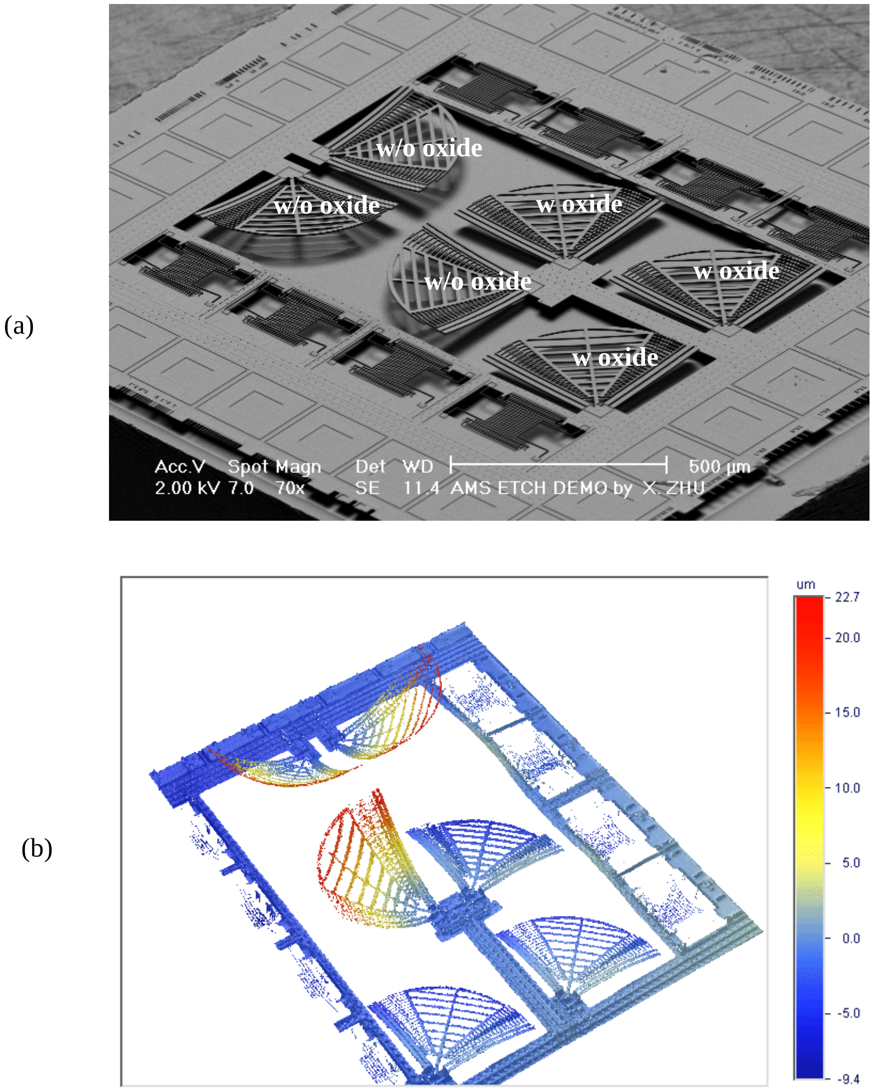

(a)
w/o oxide
w/o oxide
w oxide
w/o oxide
w oxide
w oxide
Acc.V Spot Magn Det WD 500 µm
2.00 kV 7.0 70x SE 11.4 AMS ETCH DEMO by X. ZHU
(b)
um
22.7
20.0
15.0
10.0
5.0
0.0
-5.0
-9.4

Figure. 4-14. **Removing of field oxide dramatically reduce the curling of the structures. The Wyko/ Veeco® white light interferometer measurements (b) demonstrated the removing of field oxide, by put an active layer underneath the devices (a), dramatically reduced the device curling.**

layer. An example of the curling of structures with and without field oxide is shown in Figure 4-14.

The second observation is that all the metal layers should have same width in the layout, as cross-sections shown in Figure 4-15(a). The encapsulation of metal layers underneath the mask layer is unnecessary, as in Figure 4-15(b), because the top metal layers are exposed to the plasma etching environment longer than the rest of layers and are most susceptible to process effects. Furthermore, structures that encapsulate underlying metal layers are more prone to lateral curling due to the inter-metal-layer misalignment in the CMOS process. The ion milling during the RIE narrows the structures, and strips the sidewall oxide to some extent. Therefore, structures with equal width for all the interconnect metal layers have straighter sidewalls because there is no continuous oxide on the sidewall, as shown in Figure 4-15(c). Whereas, the encapsulated layout definitely leaves the continuous oxide on the sides of structures (Figure 4-15(d)), and if they are not symmetric, lateral curling appears.

4. 6 IMPROVEMENT FOR THE FUTURE TESTING STRUCTURES

From the measurement data, design rule curves have been projected. Future design-rule test structures should therefore be available with more resolution around these curves. Testing points far away from the design rule, *e.g.* 15 % on either released side or unreleased side, can be abandoned. In this way, the entire range of each design rule is covered with a high resolution whereas the total number of structures to be measured is reduced.

The etch pit around the plate need be reduced in size in order to eliminate the effect of

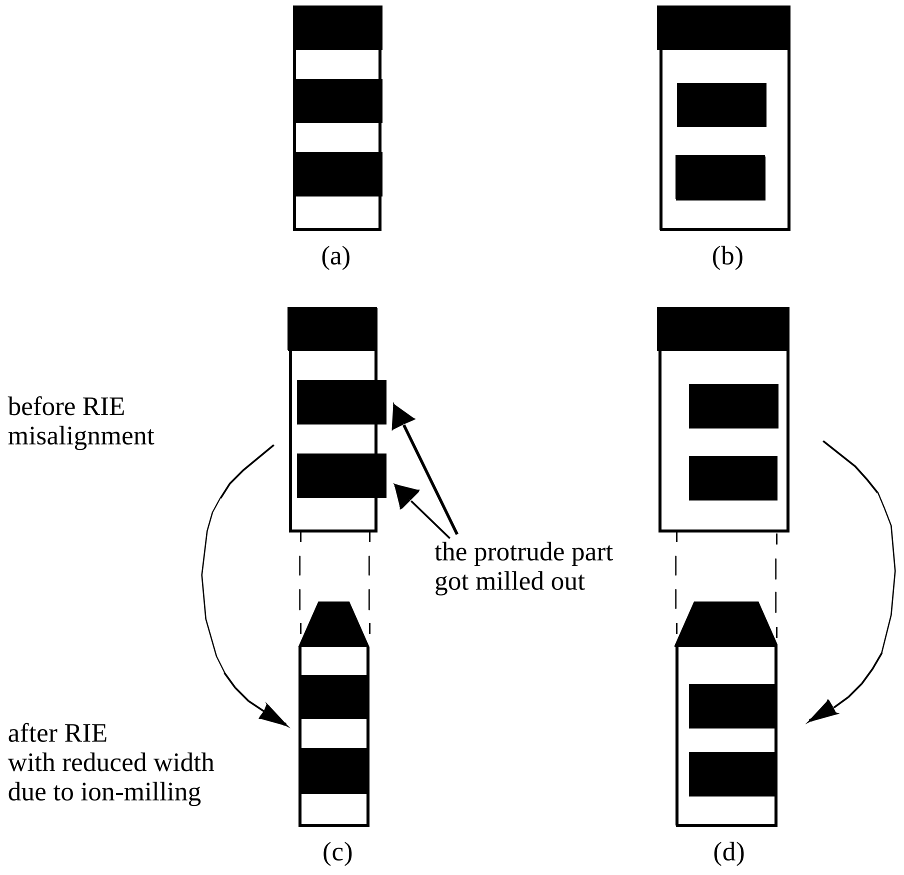
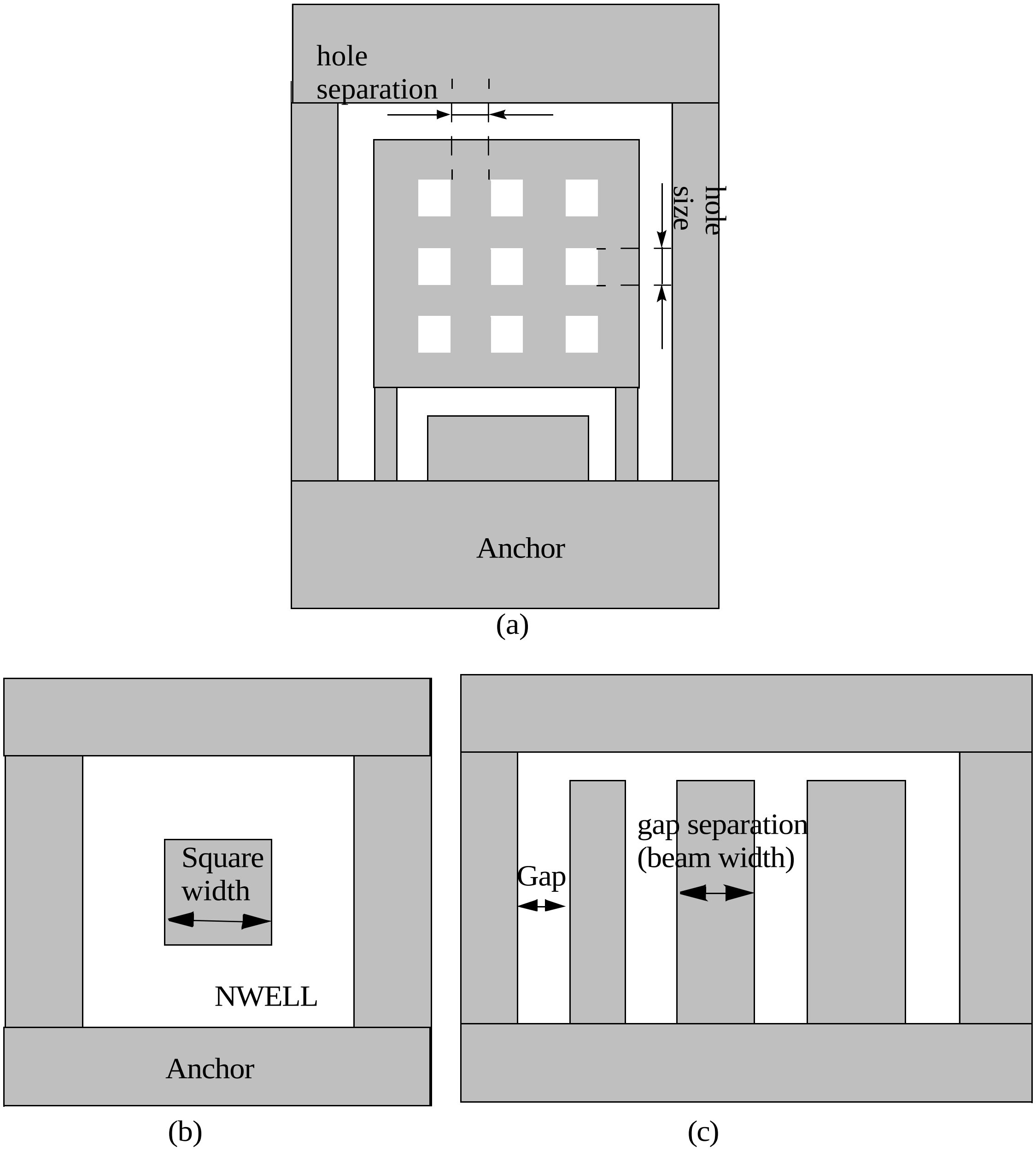


Figure. 4-15. **Beam layout effects.**
(a) Recommended layout of metal 1-2-3 beam.
(b) Layout with encapsulated metal-1 and metal-2 layers.
(c) and (d) illustrate the ion-milling effects causes narrowing of the structures. (c) shows that this effect removes sidewall dielectrics and can compensate for the misalignment in CMOS fabrication to some extent. However, for the case in (d), the resulting structure is still not symmetric, and it curls laterally.

the undercut from the periphery of the structure, as illustrate in Figure 4-16(a). In this way, the size of the plate can be reduced and more accurate etch data can be obtained. The width of the surrounding etch pit is set to the size of hole for the second generation of test structures. Only one square test pattern is used in Figure 4-16(b) instead of four in Figure 4-5(a). Also, the gap undercut structure rule is designed that in each group, the gap stays the same whereas the separation of gaps varies. This yields more compact designs.


hole
separation
hole
size
Anchor
Square
width
NWELL
Anchor
Gap
gap separation
(beam width)

(a)

(b)

(c)

Figure. 4-16. Schematic drawing shows the second generation layout
(a) The modified layout for the release hole on the plate. The width of surrounding etch pit is equal to the hole size.
(b) The modified layout for the square test structure. Only one square pattern is needed.
(c) The modified layout for the release gap test structure. With the same size of beam in the test cell, the gap separation is varied according to the first-generation design-rule test structure results.

5

Practical Issues in Post-CMOS Micromachining

5. 1 INTRODUCTION

The previous chapters describe post-CMOS micromachining step by step and focus on the methodology of finding and determining the processing space of processing parameters to fabricate MEMS structures according to the process flow described in Figure 1-1. The CMOS foundry service chosen to build MEMS devices is the Agilent 0.5 μm CMOS process [77]. The chip size is usually less than 2 mm × 2 mm, or at least one side of the chip is less than 2 mm [79]. However, the variation in processes, the modification of process modules in foundry services, the difference in CMOS processing between different CMOS providers, and advances in the CMOS fabrication technology (*e.g.* replacing Al by Cu and SiO_2 by low-K dielectric material to improve circuitry performance), all impact on the post-CMOS process flow. Some of these issues cause minor adjustments of the process, *e.g.* the process time, whereas, others require major changes in the post-CMOS process parameter settings. Extra process modules may be introduced into the post-CMOS process due to aforementioned varieties and different requirements on mechanical structures. Furthermore, as the process development becomes mature, a wafer-scale process is required for manufacturability in production. Dicing and packaging issues should also be considered, since they determine whether the production of MEMS devices is commercially feasible and profitable.

Several technical details are important but can not be easily integrated with previous chapters. The first topic is inserting a wet clean process module in the process flow to remove of residues generated by the RIE dry etch. The second topic demonstrates the migration of post-CMOS micromachining from an Al-SiO_2 CMOS foundry service to a Cu low-K CMOS process. This migration requires significant adjustment of process parameters. The third topic is the discussion of a wafer-level post-CMOS micromachining process. Compared with micromachining on small chips, Al metal mask loading and micromasking effects are significant at the wafer level. Al micromasking causes the etch rate of SiO_2 to drop down to almost zero and inhibits the following Si etch steps. Therefore, a modified process approach is required, with attentions to the special characteristics of MEMS device layout and which can achieve same goals in each process steps.

5. 2 REMOVAL OF RIE RESIDUES

Residues or etch by-products are commonly observed in CMOS processes, and are associated with different process steps in the fabrication. In general, there are three major types of residues: RIE residues, photoresist residues and CMP residues. In post-CMOS micromachining, the removal of RIE residues is related to the quality of microstructures.

During the post-CMOS micromachining process, small particles form on the top of mask layers, as in Figure 5-1(a) and a thin layer of polymer coats vertical sidewalls of

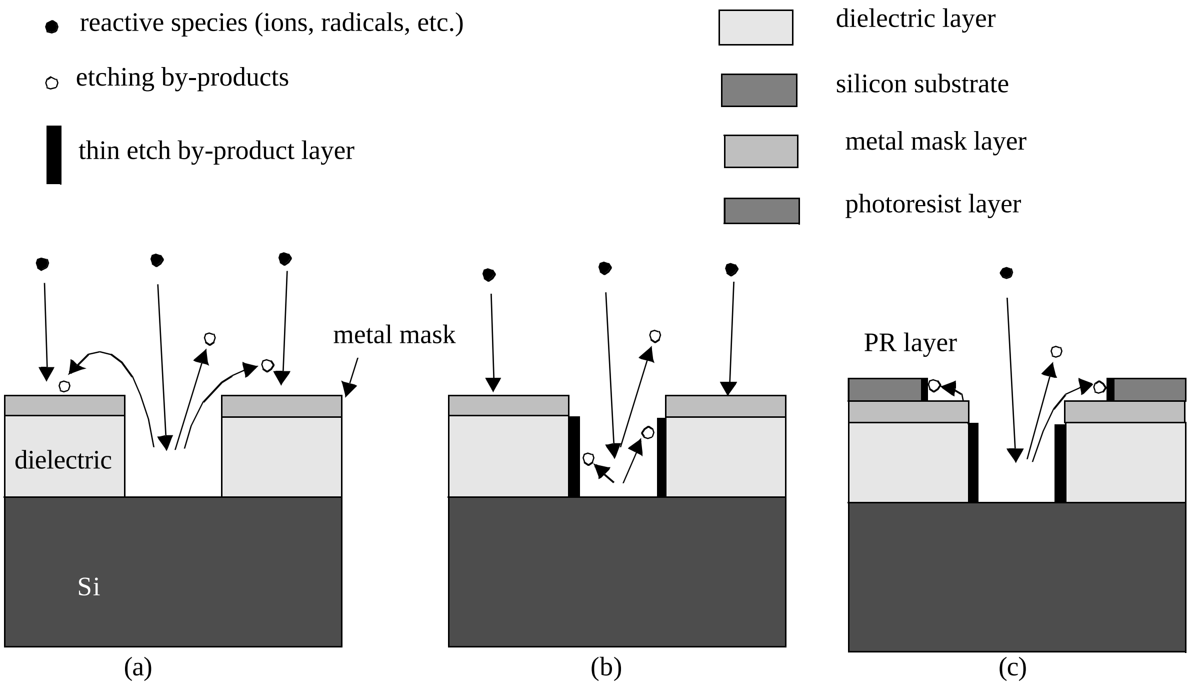

reactive species (ions, radicals, etc.)
etching by-products
thin etch by-product layer
dielectric layer
silicon substrate
metal mask layer
photoresist layer
metal mask
dielectric
Si
PR layer
(a)
(b)
(c)

Figure. 5-1. **Different sites where the residue layers or particles can be formed.**
(a) On top of mask layers.
(b) On the sidewalls of etched features.
(c) On the sidewalls of mask layers.

MEMS features, as in Figure 5-1(b). These residues occur most prominently at the dielectric layer etch step because it has the longest etch time in the entire process flow. Residue layers have even been observed on vertical sidewalls of the optional second mask layer which covers the post-CMOS MEMS metal mask layer, as in Figure 5-1(c). The corresponding SEMs are shown in Figure 5-2. These residues are generated by etch by-products in the dielectric layer etch: Si-F radicals due to the F-based plasma etching SiO_2, re-sputtered Al atoms due to high energy ions impinging on the metal mask surface, and the most important, Al-F-Si radicals which are formed by the combination of re-sputtered Al atoms and the Si-F radicals. The Al-F-Si radicals form a polymer layer which exists everywhere on samples being processed. An EDX (Energy Dispersion X-ray) analysis confirms major compounds of this polymer layer, as seen in Figure 5-3. The major peaks shows

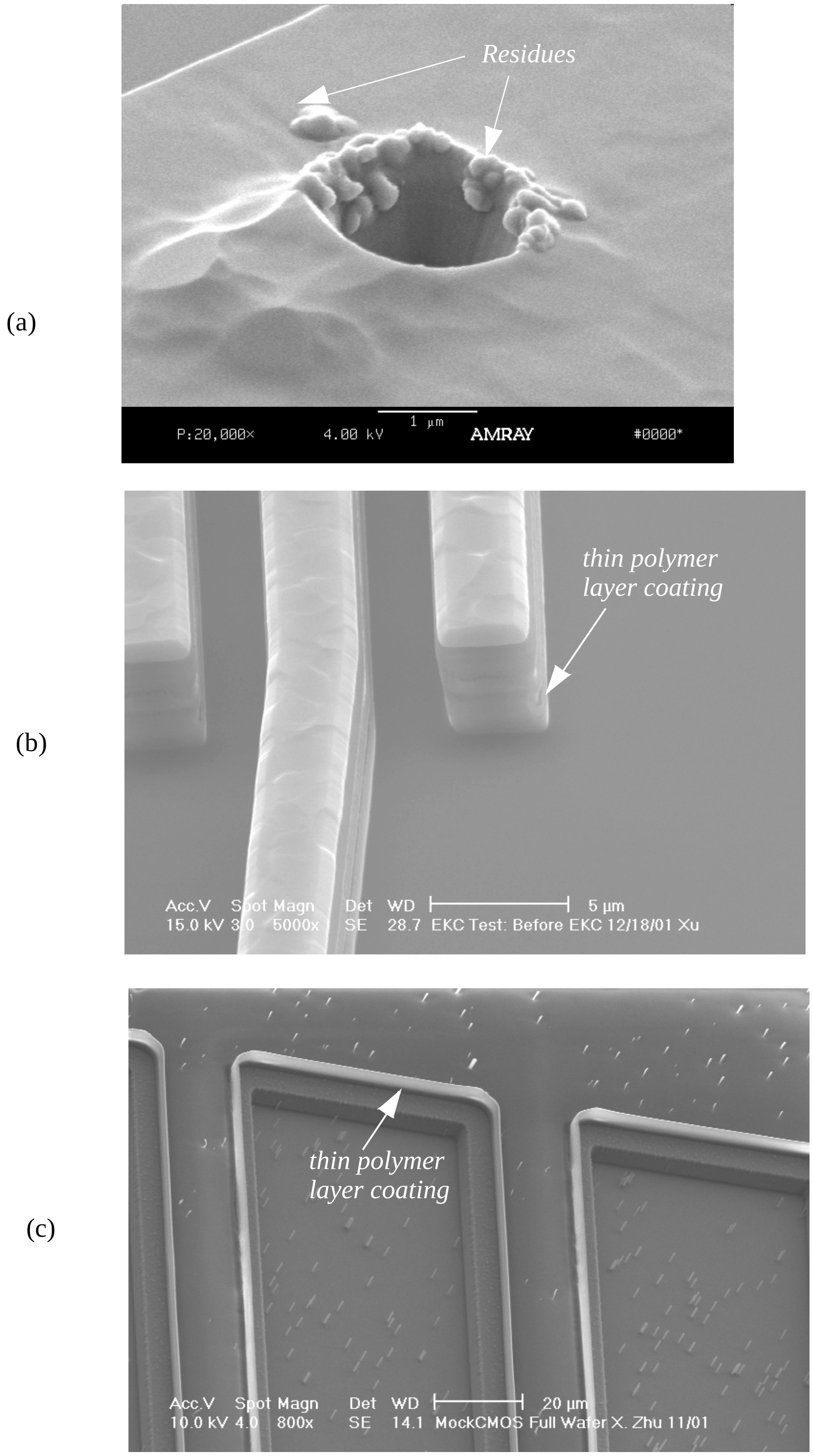

(a)
Residues
P:20,000×
4.00 kV
1 µm
AMRAY
#0000*
(b)
thin polymer layer coating
Acc.V Spot Magn Det WD 5 µm
15.0 kV 3.0 5000x SE 28.7 EKC Test: Before EKC 12/18/01 Xu
(c)
thin polymer layer coating
Acc.V Spot Magn Det WD 20 µm
10.0 kV 4.0 800x SE 14.1 MockCMOS Full Wafer X. Zhu 11/01

Figure. 5-2. **SEMs of residues on structures after an 120 min dielectric etch.**
(a) On top of mask layers.
(b) On the sidewalls of etched features.
(c) On the sidewalls of mask layers.

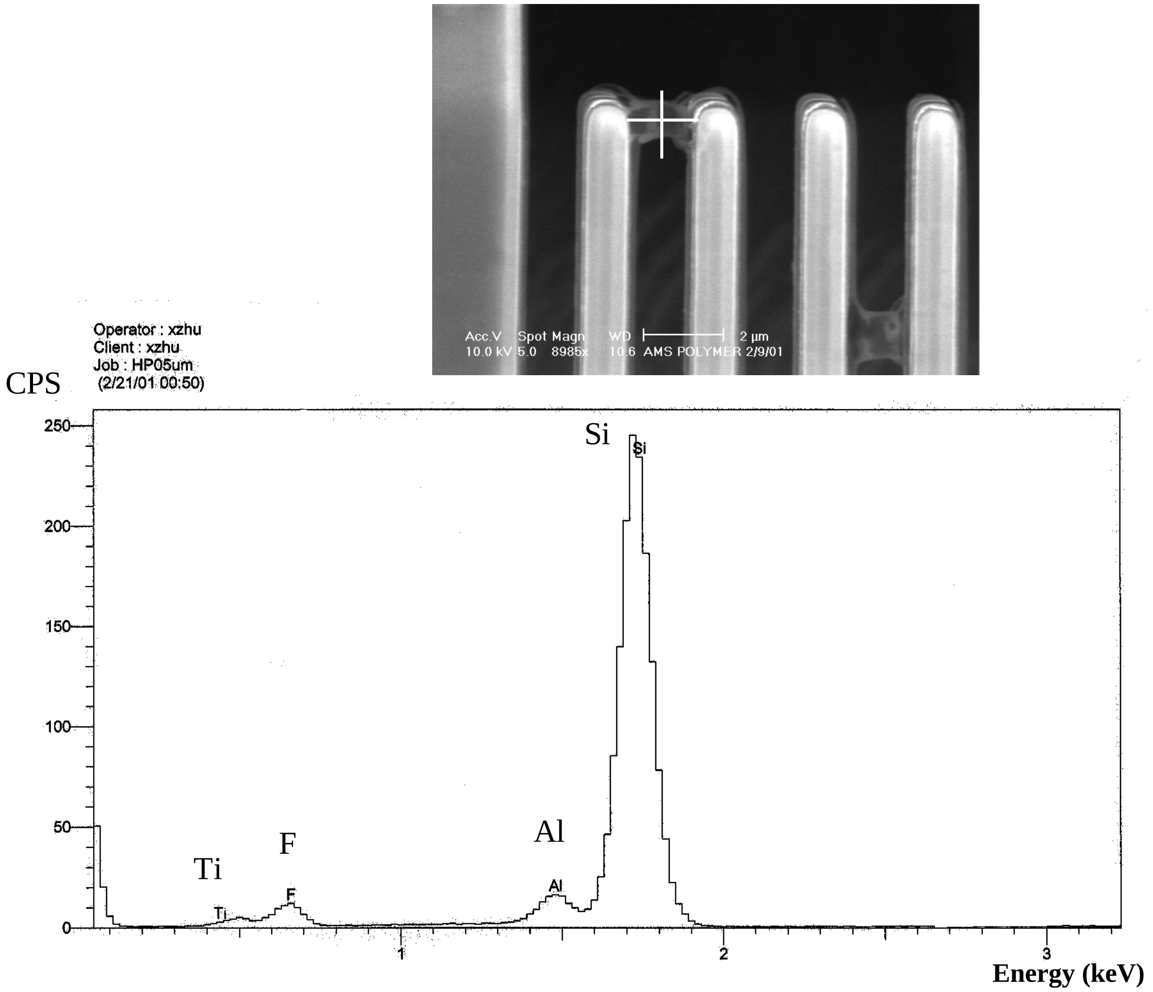


Figure. 5-3. **An EDX analysis of polymer composition. The cross-hair in the top SEM shows the sampling point. The CPS (count per second) value indicate the relative concentration of each atoms in the sampled area.**

existing of Al, F and Si. Due to the limitation of the equipment, the existence of the carbon (C) element can not be determined.

High energy ions impinge on the top surface and they remove most of the polymer. Only small portions are left while most of the area is clean, as seen in Figure 5-2(a). However, polymer coated on vertical sidewalls has a very small cross section facing incoming high energy ions. Therefore, the polymer layer builds up on sidewalls after long etches, as seen in Figure 5-2(b) and Figure 5-2(c).

The existence of the sidewall polymer layers usually does not lead to failure of MEMS structures since they are very thin, less than 100 nm, whereas, the minimum feature size of MEMS structures in current post-CMOS micromachining is above 1 μm. Although the state-of-art CMOS process can produce gate lengths approaching 100 nm, the line width and line space of metal interconnects are still at the 1 μm scale due to the high-aspect-ratio constraints which satisfy the requirement of a wire to carry certain current flow (electromigration). The minimum feature size of CMOS-MEMS structures tracks the line width of the metal interconnect. However, depending on CMOS fabrication details, *e.g.* cleaning steps, CMP steps, and type of dielectric materials, sometimes the polymer layer can become thick, and prevent the movement of MEMS structures. Moreover, when the residual stress in the structure is large, polymer layers may peel off from MEMS structures, as in Figure 5-4. The resulting polymer stringers can potentially affect the MEMS mechanical performance, *e.g.* impeding the movement of MEMS strucutures.

Usually, stripping off this polymer residue is not required, but sometimes, it is mandatory to do the cleaning, when the situation in Figure 5-4 occurs. The difficulty for this cleaning is that this polymer layer can not be easily removed, either by general wet chemicals or by an Ar/O_2 plasma/RIE clean. Two factors contribute: the small cross section facing impinging ions and a strong bond of Al-F-Si-C. Acetone, isopropyl alcohol (IPA) or methanol do not dissolve this type of polymer. A over 30 min RIE and a over 30 min ICP DRIE Ar/O_2 cleaning have no noticeable effect on removing this material. An example is shown in Figure 5-5, which corresponds to the situation described in Figure 5-1(c). No

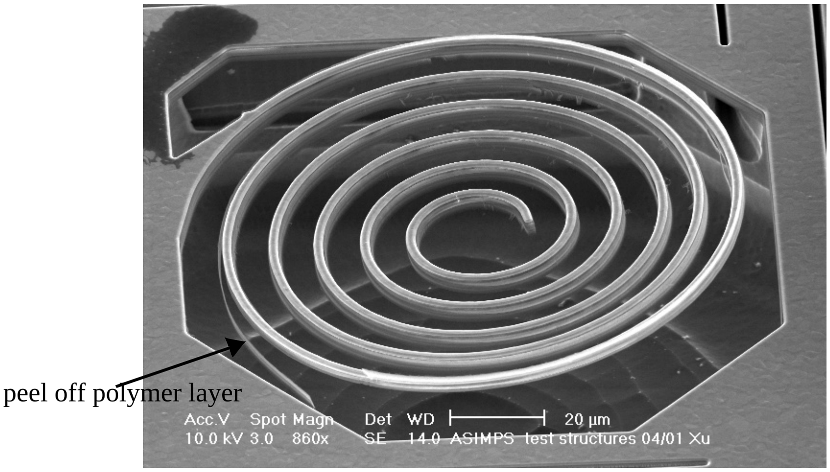

peel off polymer layer
Acc.V Spot Magn Det WD 20 µm
10.0 kV 3.0 860x SE 14.0 ASIMPS test structures 04/01 Xu

Figure. 5-4. **The polymer layer peels off from the CMOS-MEMS structure.**

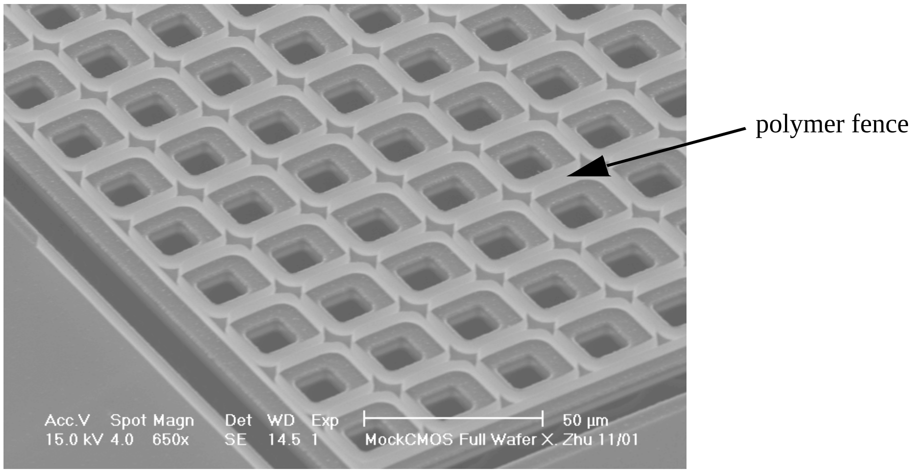

polymer fence
Acc.V Spot Magn Det WD Exp 50 µm
15.0 kV 4.0 650x SE 14.5 1 MockCMOS Full Wafer X. Zhu 11/01

Figure. 5-5. **The polymer layers coated on the sidewalls of photoresist are not affected after the photoresist being stripped out by acetone, water flushing, a 30 min Ar/O_2 plasma cleaning.**

noticeable change is observed for the fence structures with round corners in Figure 5-5 after all cleaning method aforemetioned.

Referring to experiences in semiconductor processes [80], we believe this type of polymer residue is similar to residues generated by dielectric dry etching with C-F based gas in CMOS fabrication. With the assistance from EKC Inc. [81] and Ashland-ACT Inc. [82], different types of dry-etch residue remover, which are currently used in CMOS fabrication, have been evaluated on post-CMOS processed samples. The criteria for choosing residue strippers are that the residue remover should not significantly etch metal interconnect layers, TiW barrier/ARC layers and SiO_2 dielectric layers, and at the same time, should be able to efficiently remove the polymers. Five types of strippers have been identified at company side which can achieve the our goals. Their name and operation conditions are listed in Table 5-1.

Table 5-1: Identified Residue Remover for the Post-CMOS Process Application

Company	Product Name	Operation Temperature(°C)	Time (min)	Processing Container
EKC technology	EKC6800	25	40	Teflon
	EKC640	25	20	Teflon
	EKC325	75	30	Teflon
Ashland ACT	NE-87	25	30	Teflon
	NE-88	25	30	Teflon

Although the chemical composition is a trade secret and the mechanism of removing polymer is not quite clear, we guess that the chemical may slightly dissolve residue material, penetrate Al-F-Si-C residue layers, reach the inter-surface between polymer residues and SiO_2, slightly etch the SiO_2 surface and make polymer films peel-off from the structure sidewall. The cleaning results are shown in Figure 5-6. It is obvious that dry etch residues, which are on the top of metal mask surface and encapsulate sidewalls of MEMS structures, have been removed. Multilayer structures are clearly exposed, as illustrated in the right column of Figure 5-6.

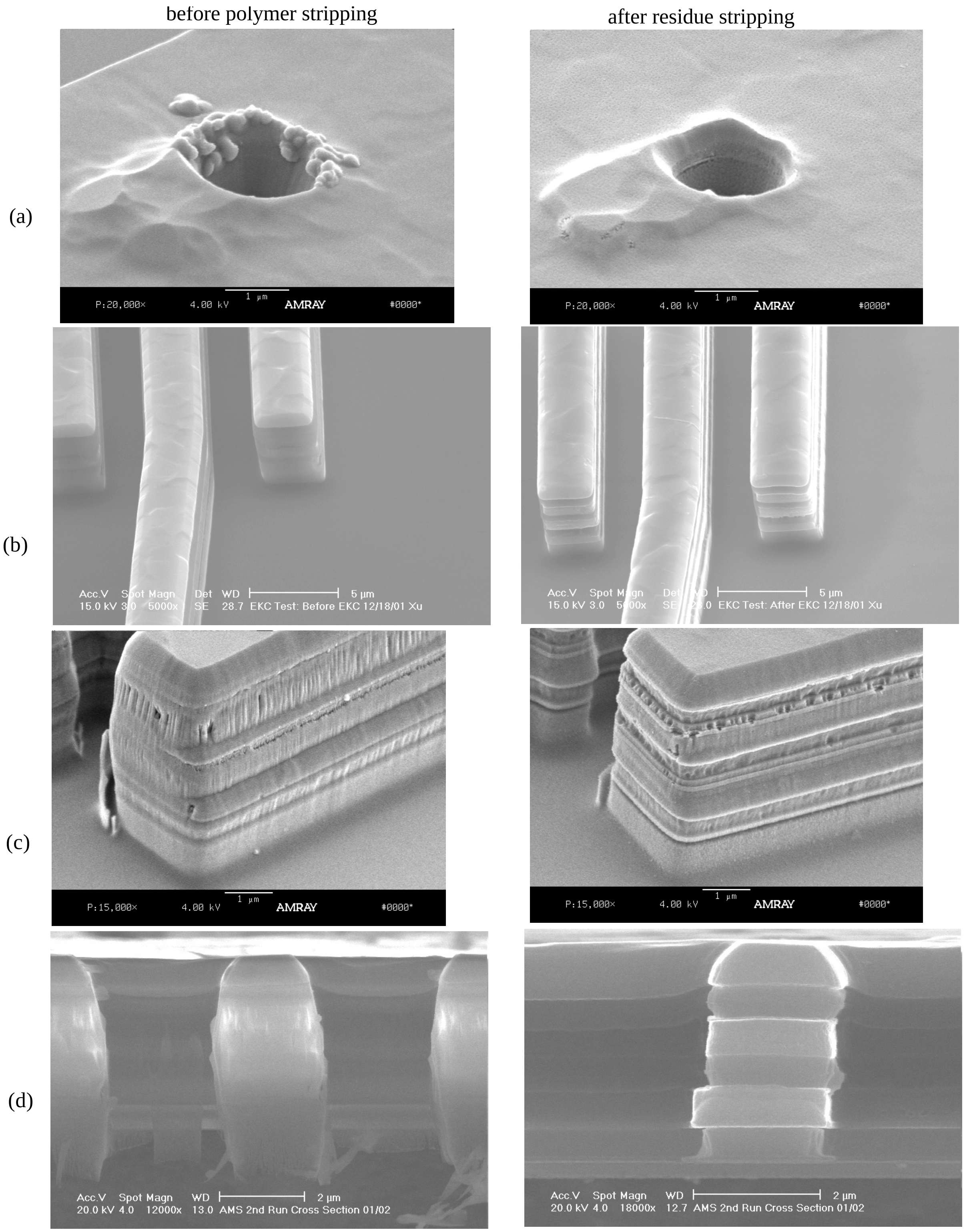

before polymer stripping
after residue stripping
(a)
P:20,000× 4.00 kV 1 µm AMRAY #0000*
P:20,000× 4.00 kV 1 µm AMRAY #0000*
(b)
Acc.V Spot Magn Det WD 5 µm
15.0 kV 3.0 5000x SE 28.7 EKC Test: Before EKC 12/18/01 Xu
Acc.V Spot Magn Det WD 5 µm
15.0 kV 3.0 5000x SE 28.0 EKC Test: After EKC 12/18/01 Xu
(c)
P:15,000× 4.00 kV 1 µm AMRAY #0000*
P:15,000× 4.00 kV 1 µm AMRAY #0000*
(d)
Acc.V Spot Magn WD 2 µm
20.0 kV 4.0 12000x 13.0 AMS 2nd Run Cross Section 01/02
Acc.V Spot Magn WD 2 µm
20.0 kV 4.0 18000x 12.7 AMS 2nd Run Cross Section 01/02

Figure. 5-6. **Polymer residue remover results.**
(a) On the top surface, after 30 min soaked in Ashland-Act NE-87 and before release.
(b) On the sidewalls of microstructures, after 40 min soaked in EKC6800 solution.
(c) On the sidewalls of microstructures, after 30 min soaked in Ashland-Act NE-87.
(d) On the edge of chips, 40 min soaked in EKC6800 solution on the released chip.

5. 3 MIGRATING PROCESS FROM AL-SIO_2 TO CU LOW-K DIELECTRIC

5. 3. 1 Introduction

In modern CMOS processes, interconnect delays begin to dominate overall device delays starting at 0.18 μm gate length. In order to achieve higher speed and less power consumption, which is limited by the resistance of metal wire interconnections and the capacitance between the wires, the semiconductor industry is moving from the Al interconnect SiO_2 dielectric technology to the Cu interconnect low-K dielectric process. The obvious reasons are that copper has lower resistance than aluminum and low-K dielectrics have lower capacitance than SiO_2 [83]. The semiconductor industries have already switched to the copper process after years of the research and the development. IBM has switched the interconnect in their PowerPC microprocessor to copper interconnect since 1997 [84]. Intel unveiled Cu interconnect in their Northwood Pentium 4 processor in January 2002 [85]. By developing post-CMOS micromachining for the Cu low-K processes, MEMS devices can take advantage of the high conductivity and electromigration of Cu and of multilayer interconnections. High quality factor passive components for RF system-on-chip are good applications to this technology.

A six-layer interconnect in UMC 0.18 μm Cu Damascene processing is shown in Figure 5-7. Instead of using Al interconnect layers as a mask layer in the dielectric structural etch, the top-most Cu layers delineate microstructures. Challenges exist when migrating post-CMOS processing from Al-SiO_2 interconnect CMOS to Cu low-K interconnect CMOS. As an etch resist mask material, Cu is harder to RIE dry etch than Al even though Cu is a softer material, doubling in sputter yield [86]. Compared with the RIE dry

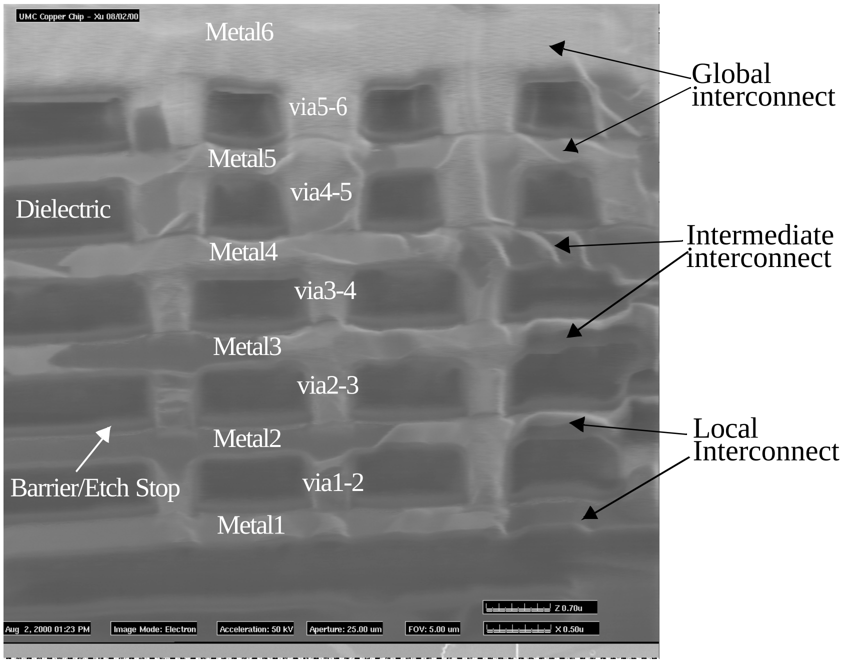

UMC Copper Chip - Xu 08/02/00
Metal6
Global interconnect
via5-6
Metal5
via4-5
Dielectric
Intermediate interconnect
Metal4
via3-4
Metal3
via2-3
Local Interconnect
Metal2
Barrier/Etch Stop
via1-2
Metal1
Z 0.70u
Aug 2, 2000 01:23 PM
Image Mode: Electron
Acceleration: 50 kV
Aperture: 25.00 um
FOV: 5.00 um
X 0.50u

Figure. 5-7. **Six-layer interconnect in a Cu Damascene process with Cu vias by UMC.**

etch of dielectric layers on Al and Cu interconnect chips, the etch rate of the Cu mask is 20 % that of Al in a Plasma Therm 790 chamber with CHF_3 flow at 22.5 sccm, O_2 flow at 16 sccm, processing pressure at 125 mT, DC bias 340 V and plasma density 0.55 W/cm^2. The explanation is that the reaction product of the Cu is not volatile. However, it is still important to control the power of RIE to prevent the re-sputtering of Cu onto the dielectric surface.

The low-k dielectrics generate problems of adhesion and reliability of microstructures. For example, Novellus fluorinated oxide (FSG, k=3.6) [87] is a fluorine enriched dielectric material. It is deposited by PECVD or HDP-CVD tools, adding silicon tetrafluoride (SiF_4) to silane (SiH_4), O_2 and argon gases [83]. The high electronegativity of fluorine atoms reduces the polarizability of the SiO_2 film, thus decreasing the dielectric constant. The downside is that fluorine may evolve from the oxide, and etch Ta/TaN/TiN barrier layers that exist to inhibit Cu diffusion into dielectric insulators. Even though the FSG can be etched as an undoped oxide, the fluorine may break the bond in the CVD film or may be generated from plasma disassociation and etch the barrier layers. This effect can cause delamination of metals in microstructures in Cu chips, as shown in Figure 5-8, which is not seen in normal Al-SiO_2 microstructures. With understanding of each process parameter's influence [60], the delamination issue is solved with a penalty of 50% reduction of etch rate. Doubling the O_2 flow rate and reducing the chamber pressure by 50% enhance ion bombardment and reduces fluorine reaction with the barrier layers, as reported in [88].

Erosion of the Cu layer, shown in Figure 5-9, is another issue and occurs after prolonged exposure of the Cu surface to moisture in the ambient. We hypothesize that fluo-

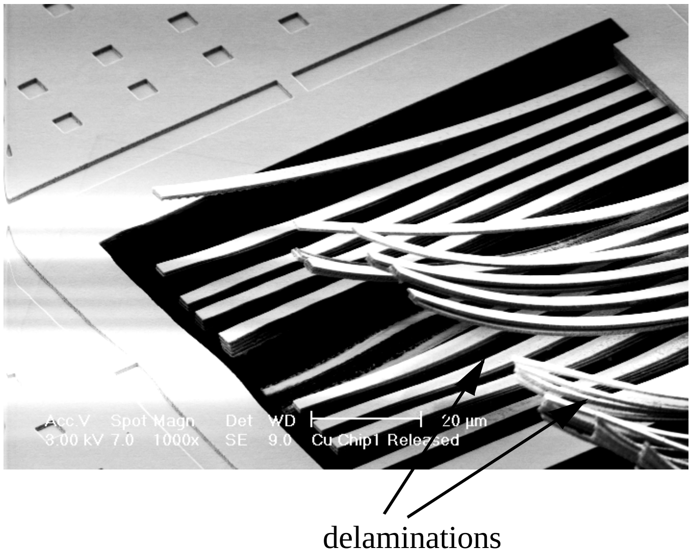

Acc.V Spot Magn Det WD 20 µm
3.00 kV 7.0 1000x SE 9.0 Cu Chip1 Released
delaminations

Figure. 5-8. **Delamination of the mechanical structures with the post-CMOS Al-SiO_2 microstructure etch recipe. The extra fluoride in the low-K dielectric causes severe delamination.**

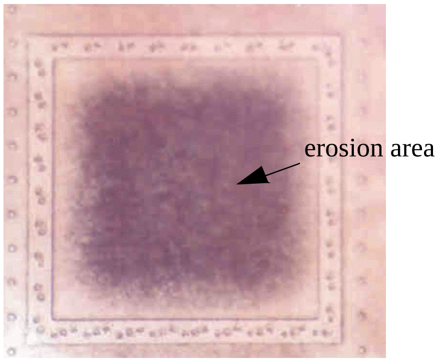


Figure. 5-9. **The effects of corrosion on the exposed copper surface. Shown here is a pad after 2 days exposed to the ambient.**

ride-rich residues left from the etch produce acids when they are exposed to moisture of the environment, and cause corrosion in Cu. Such action is not seen in the Al post process due to a protective insulating aluminum oxide film that forms during the process to encase the exposed Al. Ar cleaning or IPA rinse after the dielectric etch significantly increases the Cu resistance to the erosion. Argon plasma after device releasing also helps in removing residues on MEMS structures. Minimizing the exposure of MEMS device to moisture after the dielectric etch and immediately continuing on the next DRIE Si trench etch step reduces the erosion of the Cu surface due to the less absorption of the water and the removal of the dielectric etch residue by the DRIE ICP plasma. Devices after all micromachining steps show no erosion after accelerated aging in a humidity chamber (90% humidity, 70°C) for 24 hours. The erosion rate of Cu after the process was evaluated by four-point resistance measurement of a planar inductor coil, which reflects the sheet resistance change of Cu. A typical accumulated erosion curve is shown in Figure 5-10. The first 20 hours contributes to most of the erosion followed by a much slower rate later. This is probably due to the fluorine-rich residue being thoroughly reacted with the Cu and not avail-

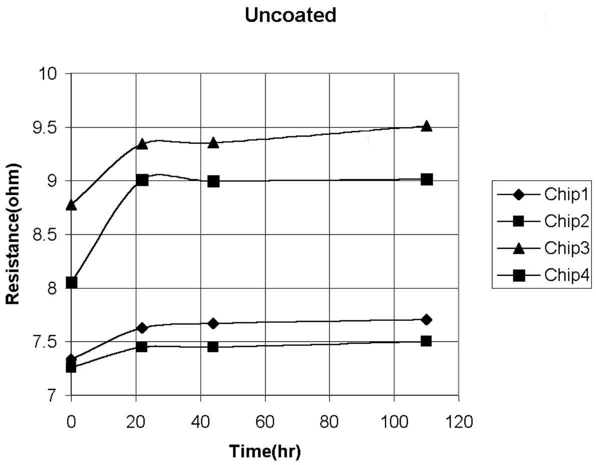


Figure. 5-10. **Four-point measurement of the inductor resistance change (an indication of sheet resistance change) vs. the time of the inductor in the humidity chamber.**

able for more etching on the surface. This is partially confirmed with the observation of chips without the cleaning procedure or coated with fluorine-rich polymers. The erosion doesn't stop on these samples even after 200 hours in humidity chamber, although with a much slower rate. The correct coating material not only has to encapsulate the MEMS structures but also must not contain any chemistry which could react with Cu.

The complete process details on post-CMOS micromachining on Cu interconnect low-K dielectric chips are available in Appendix A.

5. 3. 2 Material Properties

The curling measurements were made on two types of beams. One is made with field oxide as the most bottom layer and the other has only low-K dielectric in its entire composition. Each beam is 100 µm in length and 3.3 µm in width. The measurements were made using a interferometric optical system and are summarized in Table 5-2. The least curled

Table 5-2: Out-of-plane tip deflection for Cu low-K dielectric beams 100 mm-long 3.3 mm-wide (unit: mm)

Beam Type	w/field oxide	w/o field oxide
M1-2-3-4-5-6	0.13	0.39
M2-3-4-5-6	1.17	1.04
M3-4-5-6	1.3	1.56
M4-5-6	1.56	1.56
M5-6	1.4	1.04
M6	0.52	0.78
M1-2-3-4-5	0.39	1.04
M1-2-3-4	1.62	2.86
M1-2-3	1.8	3.12
M1-2	5.98	7.3
M1	>9	>9

beam in the Cu process has a vertical tip deflection of 0.13 μm while that of the Agilent 0.5 μm Al interconnect process is about 1.5 μm.

The Young's modulus of the beam was obtained by measuring the resonant frequency of 130 μm long, 1.9 μm wide beams. The mechanical resonant frequency of a single cantilever beam is given by [89]:

$$f_{res} = 0.56\sqrt{\frac{Ew^2}{12\rho L^4}} \tag{5.1}$$

where, E is the Young's modulus, w is the width of the beam, L is the length, and r is the effective density of the beam. If a weighted average of the copper and oxide is taken to compute the effective density [90], the Young's modulus is then fitted to the measurement of resonant frequency. The results are listed in Table 5-3.

Measurements were taken of mechanical frequency response of a Cu low-K dielectric crab-leg resonator, shown in Figure 5-11, which is an identical design to a prior test struc-

Table 5-3: **Young’s modulus of Cu low-K dielectric beams (unit: GPa)**

Beam Type	Young’s modulus
M1-2-3-4-5-6	91.6
M1-2-3-4-5	93.5
M1-2-3-4	91.6
M6	62

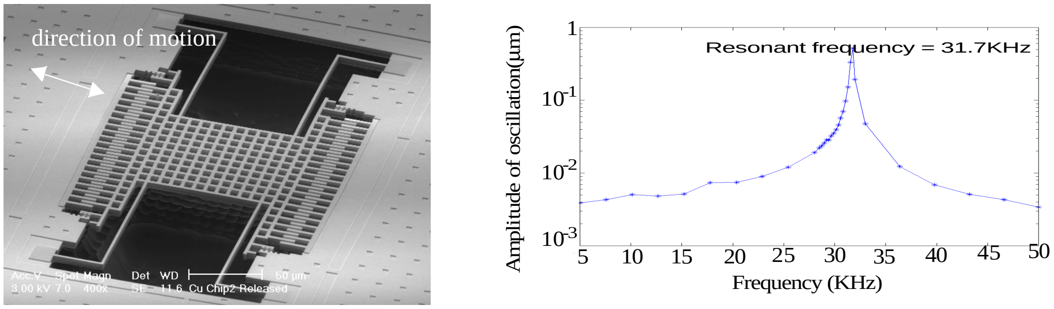


Figure. 5-11. **Measurement of MEMS structures built in UMC Cu interconnect low-K dielectric process.**
(a) Crab-leg resonator in Cu low-K dielectric interconnect process.
(b) Frequency response of the crab-leg resonator, with 4VDC+4VAC driving voltage.

ture in the Agilent 0.5 µm process. The Cu resonator has a mechanical quality factor of 70 at a frequency of 31.7 kHz in the air. The aluminum structure has a resonant frequency of 41.5 kHz with a mechanical quality factor of about 40. The reduced resonant frequency is due to the higher density of the Cu.

5. 4 WAFER-LEVEL POST-CMOS MICROMACHINING PROCESS

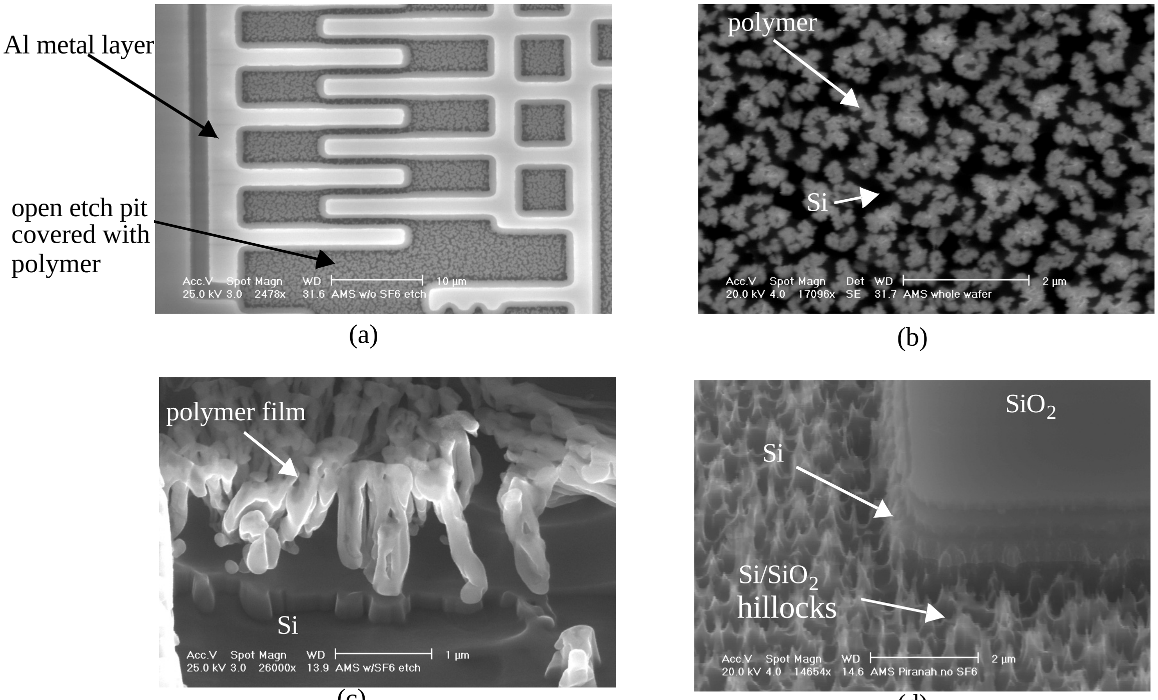
5. 4. 1 Introduction

As post-CMOS micromachining matures, wafer-level fabrication to support volume production becomes necessary. Previous results [31][60][91] were obtained using CMOS metal interconnects as an etch resist mask on small samples, usually 2 mm × 2 mm. Advances in CMOS lithography enable precisely defined microstructures, and metal layer combinations allow various structure heights. However, when a full wafer is processed, the dielectric etch ceases and the surface becomes very rough because of micromasking induced by the large exposed area of metal. Although it has been reported that metal can be used as a mask in RIE dry etch process [92][94], and some research demonstrated that the metal mask can even function as a catalyst to accelerate the etch[93], the micromasking effect should be alleviated as much as possible and it should not impede the etch, especially when a long-time etch is required. We have observed the micromasking effect significantly reduces the etch rate both in the dielectric etch and in the deep Si trench etch. Therefore, exploring a modification on the process but still keeping the same concept to build MEMS structures on CMOS chips is crucial to the successful commercialization of the post-CMOS micromachining technology.

5. 4. 2 Micromasking Effects in Dielectric Etch

In the dielectric etch, a severe micromasking effect may appear, and it depends on the sample etch time and exposed metal area to the plasma.

Usually, when micromasking becomes severe during etching, a porous, grass-like film appears on the etched surface as shown in Figure 5-12, The by-products of the etch redeposit on the etched surface, form a thin-film layer, cause etch uniformity variation across the wafer and increase the surface roughness. When the spikes of the grass-like film exceed the wavelength of incoming light after some time, this light will be captured between the spikes and cannot leave the film surface anymore. Moreover, the rough surface reflects this light randomly in any direction. Therefore, the surface being etched turns black instead of shining grey under the inspection of the optical microscope. This observa-


Al metal layer
open etch pit covered with polymer
Acc.V Spot Magn WD 10 µm
25.0 kV 3.0 2478x 31.6 AMS w/o SF6 etch
polymer
Si
Acc.V Spot Magn Det WD 2 µm
20.0 kV 4.0 17096x SE 31.7 AMS whole wafer
polymer film
Si
Acc.V Spot Magn WD 1 µm
25.0 kV 3.0 26000x 13.9 AMS w/SF6 etch
SiO_2
Si
Si/SiO_2 hillocks
Acc.V Spot Magn WD 2 µm
20.0 kV 4.0 14654x 14.6 AMS Piranah no SF6

(a) (b)

(c) (d)

Figure. 5-12. **The characteristic of the Al micromasking effect under SEM.**
(a) A top view shows a grass-like porous film coated on the etched surface.
(b) A top closed look of the porous film. The shining irregular pattern is the etching by-product redeposit on the surface.
(c) A cross section of the porous film.
(d) A piranha (*e.g.* H_2SO_4:H_2O_2 = 5:1) cleaning reveals the rough surface underneath the porous film.

tion is used to monitor the micromasking effect.

The time dependence of the micromasking is illustrated in Figure 5-13. When the size of sample exceeds 2 mm × 2 mm, as etch time increases, the SiO_2 film being etched turns from shining gray, as in Figure 5-13(a), to shining in some areas and black in the other areas, and to thoroughly black in all areas after 180 min etch, where the SiO_2 film is not completely etched to the Si substrate. Figure 5-14 shows an average of five-point measured results of on the full wafer. Comparing the data in the first 60 min to the last 60 min, the etch rate is reduced by 50%.

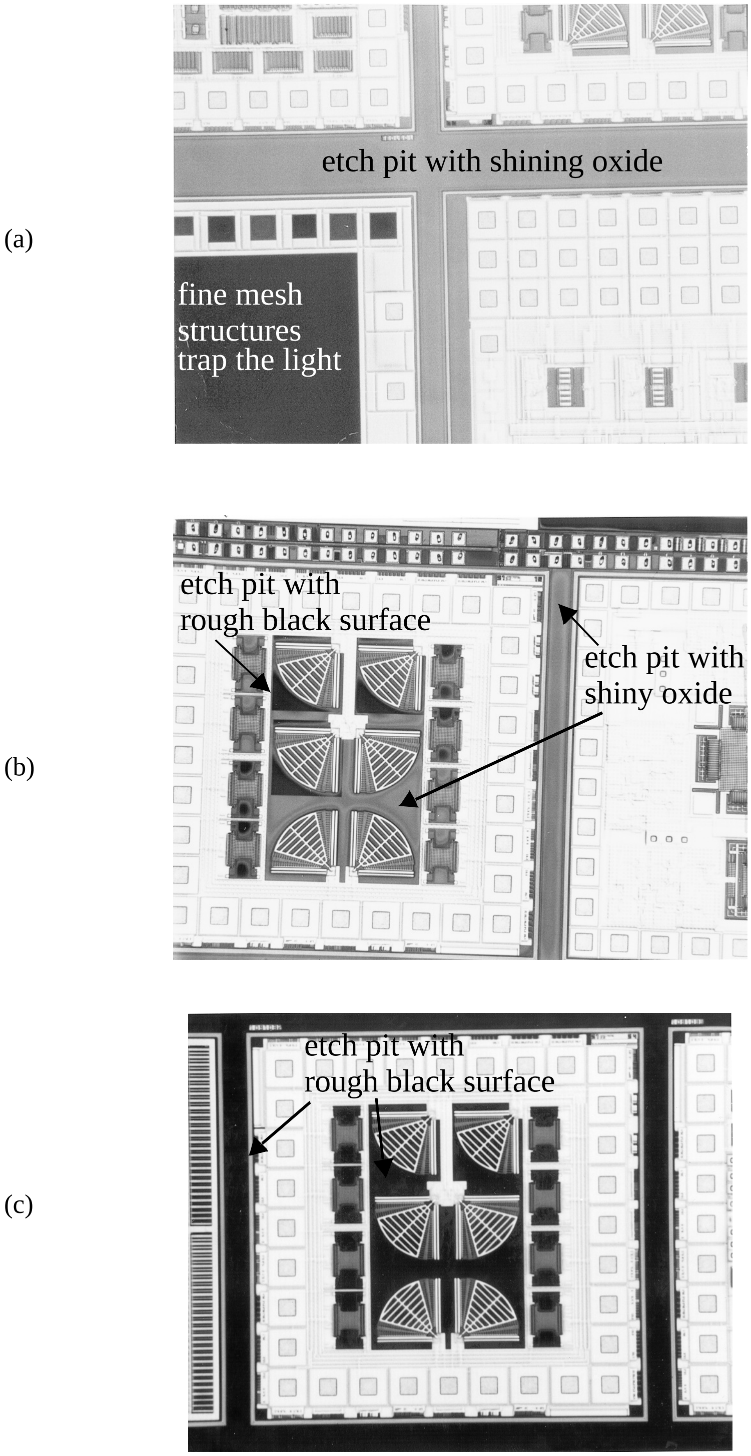

(a)
etch pit with shining oxide
fine mesh structures trap the light
(b)
etch pit with rough black surface
etch pit with shiny oxide
(c)
etch pit with rough black surface

Figure. 5-13. **Optical microscope photos indicate the severeness of micromasking effect related with dielectric etch time.**
(a) After 60 min etch, almost no micromasking effect appears on the sample surface.
(b) After 120 min etch, some area indicates the micromasking effect.
(c) After 180 min etch, the micromasking effect appears everywhere on the chip.

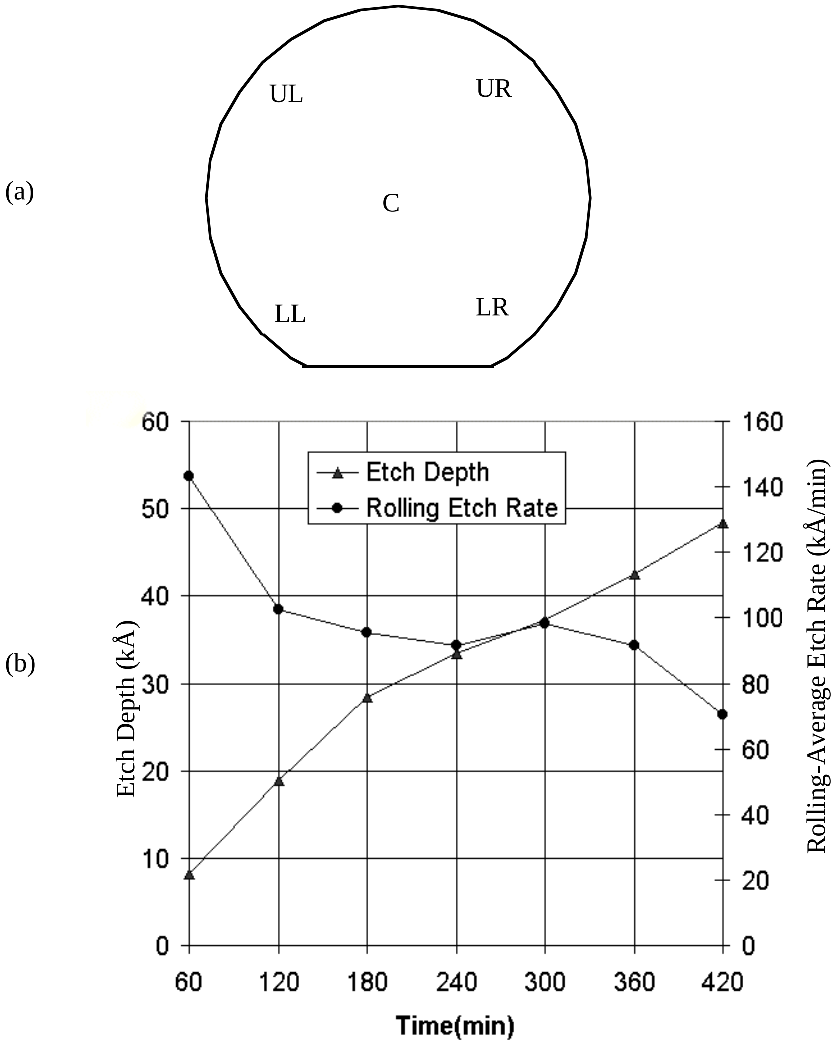


Figure. 5-14. A measurement on the slowdown of etch rate due to the micromasking effect.
(a) A map of the five-point etch rate measurement on the wafer.
(b) The etch depth and etch rate rolling-averge versus time.

The severeness of the micromasking effect is also dependent on the amount of exposed metal area. When the continuous metal mask area of the sample is less than 2 mm on either side, micromasking effects are not significant in the oxide etch, as in Figure 5-15. Above this level, the micromasking effect becomes serious.

Significant reduction in the etch rate is observed. Varying the gas ratio, pressure, or

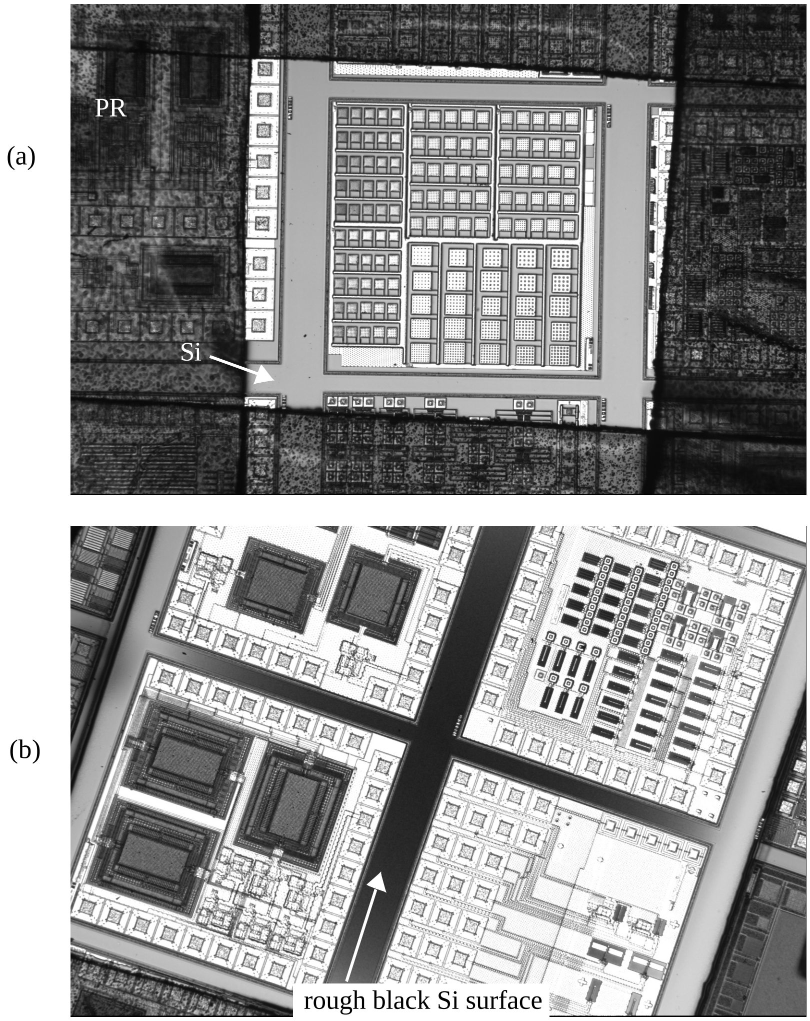


Figure. 5-15. **Demonstration of the effect of sample area on micromasking.**
(a) One 2 mm × 2 mm chip has clean surface after the etch.
(b) Four 2 mm × 2 mm chips next to each other shows the micromasking effects, resulting in rough black Si surface.

RF power around the optimized processing point does not change this situation. Even for the initial etch, *e.g.* the first 60 min etch in Figure 5-14, the etch rate with large exposed area of metal is only 65% of that with the small exposed metal area.

A CF_4/O_2 gas mixture has also been tested to etch the dielectric instead of CHF_3/O_2, which is presumed to generated more polymer. But the results, as in Figure 5-16, show no noticeable improvement on the etch.

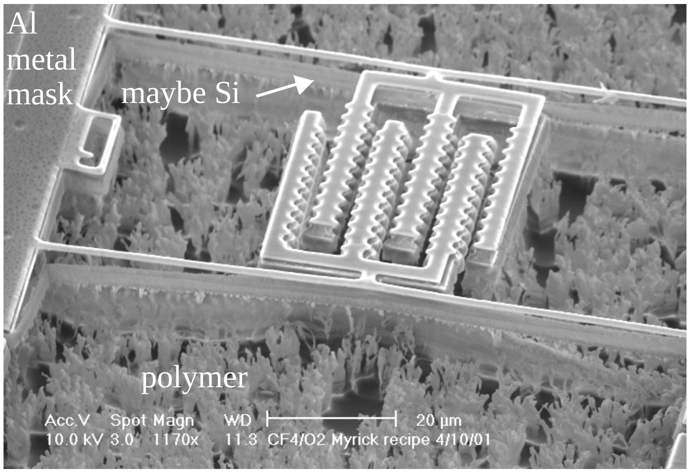


Figure. 5-16. Results from a CF_4/O_2 gas mixture dielectric etch. The CF_4/O_2 etch doesn't result in a reduction of polymer generation compared with CHF_3/O_2 processing gas.

When the micromasking effect becomes significant, polymer deposited on the sidewalls of MEMS structures will be much more thicker. It is so thick that it close the gaps between each pair of comb fingers, as in Figure 5-17(c).

The EDX on this polymer yields the same result as in the Figure 5-3, a Al-F-Si-C compound spectrum. Sometimes, Ti, an element in the barrier/ARC layer is also present. Although the following Si isotropic etch can smooth the Si surface underneath the structure, it won't dissolve the grass-like residue on the top of the Si surface, as in Figure 5-18.

Overall, if a long etch time is required for a dielectric etch as in the post-CMOS micromachining process, the idea of using metal masks to define MEMS structures is only valid when the sample size is small. For the large sample and wafer level processing, the etch ceased due to the generation of polymer film. Moreover, these thick polymer layers may obstruct the movement of MEMS structures. The hurdle of this polymer residue associated with using a metal mask needs to be overcome in the process development, and will be

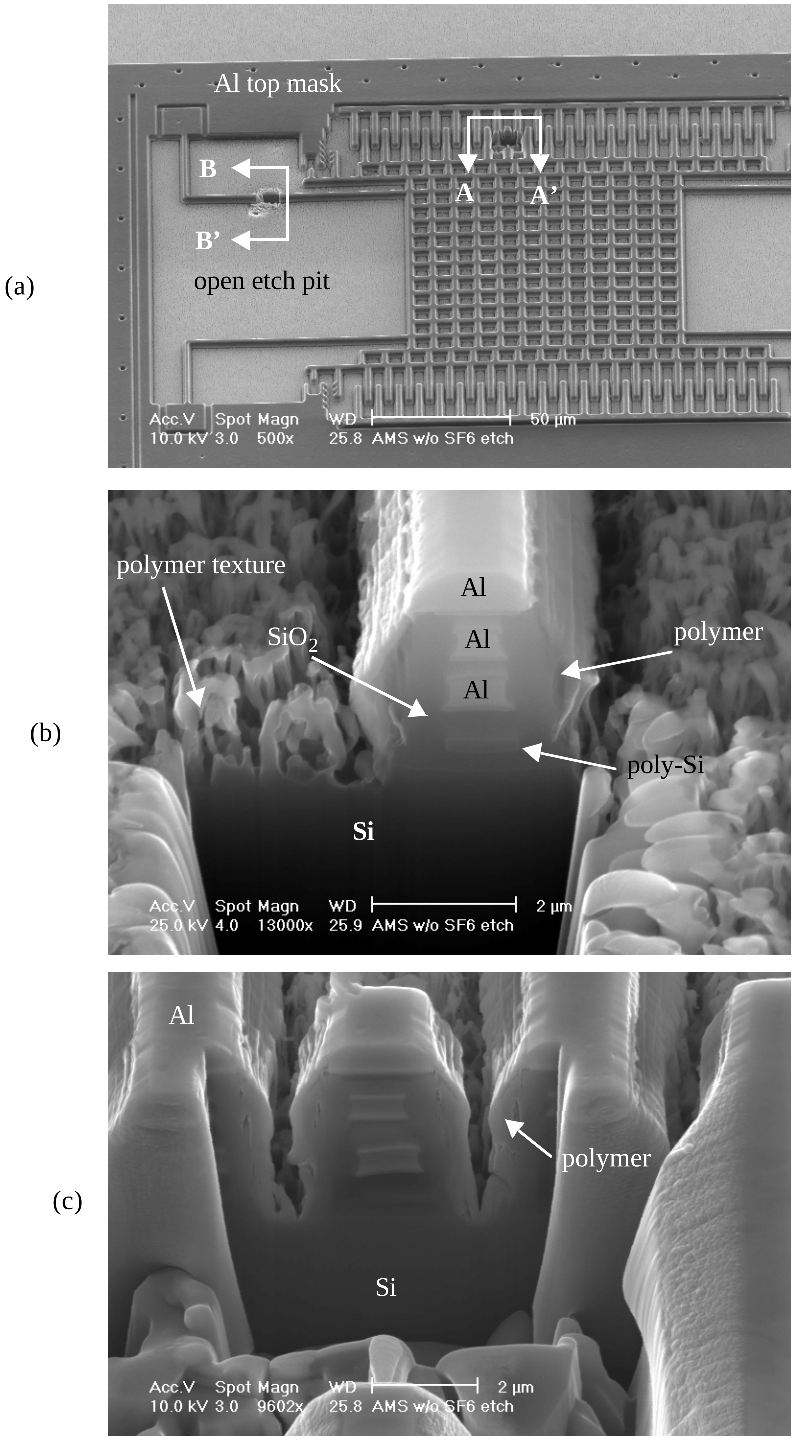

(a)
Al top mask
B
B'
A
A'
open etch pit
Acc.V Spot Magn WD 50 µm
10.0 kV 3.0 500x 25.8 AMS w/o SF6 etch
(b)
polymer texture
Al
Al
Al
SiO2
polymer
poly-Si
Si
Acc.V Spot Magn WD 2 µm
25.0 kV 4.0 13000x 25.9 AMS w/o SF6 etch
(c)
Al
polymer
Si
Acc.V Spot Magn WD 2 µm
10.0 kV 3.0 9602x 25.8 AMS w/o SF6 etch

Figure. 5-17. **Thick polymer layer deposition resulting from Al micromasking.**
(a) A crab-leg resonator after 140 min dielectric etch.
(b) The beam surrounded by large etched area is on the B-B' cross section in (a) above.
(c) A comb finger area where more metal is exposed, on the A-A' cross section in (a) above.

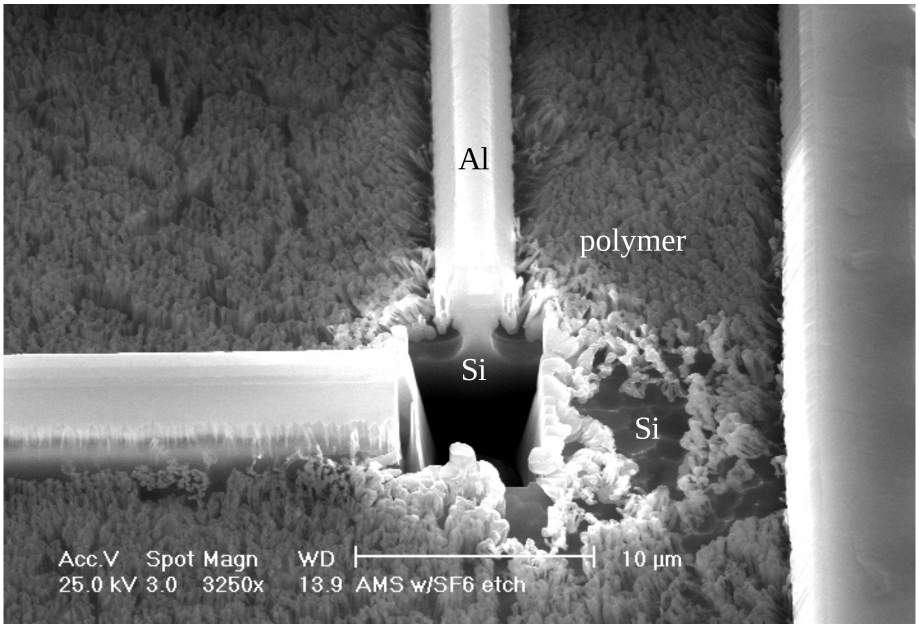


Figure. 5-18. Si isotropic etch does not dissolve the grass-like polymer residues on the top of the Si surface.

discussed in the later part of this chapter.

5. 4. 3 Micromasking Effects in Si Deep Trench Etch

As documented in the Appendix A, the microstructural release steps require a 30 min Si anisotropic etch and a 5 to 7 min isotropic etch in an ICP DRIE system [91]. Especially for the deep trench anisotropic etch step, which occupies 80% of the ICP chamber processing time, concerns arise about the degradation and contamination of the processing chamber. An ICP process usually has a very low DC bias voltage, below 100 V compared with greater than 300 V in a common RIE parallel-plate system. This low DC bias significantly reduces the re-sputtering of the metal. However, the high density ion flux, 100 times higher than a RIE system, increases the number of metal atoms being knocked out from the mask surface. To explore this issue, a series of experiments were conducted on 4-inch wafers in an STS system.

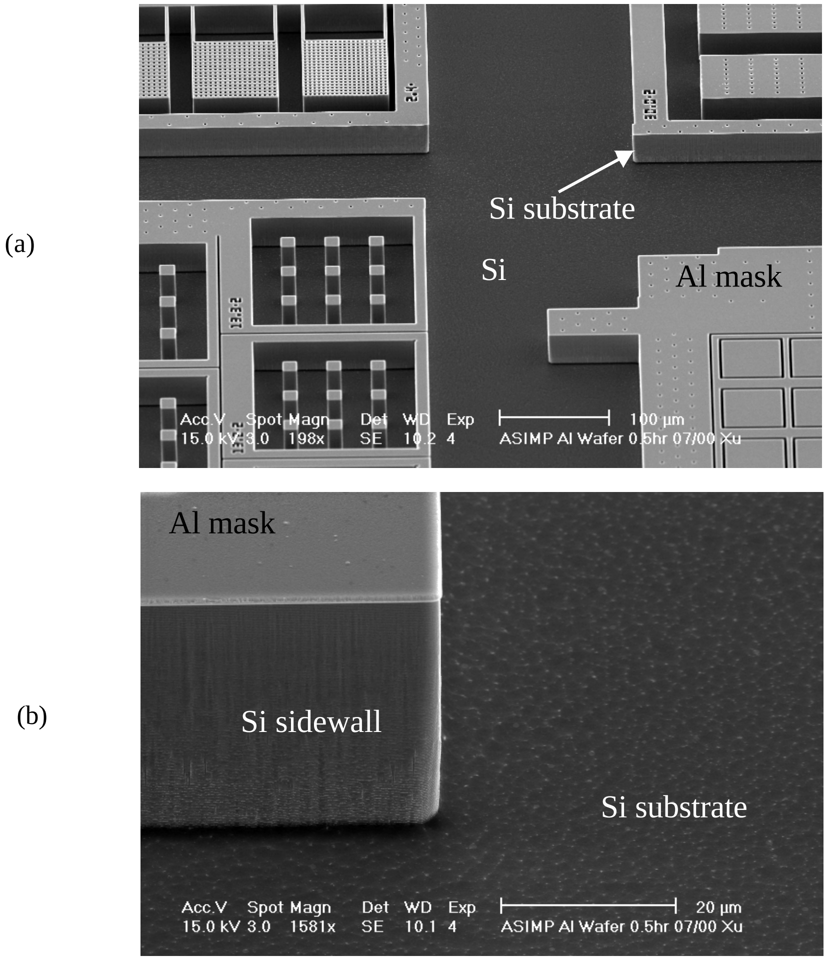

(a)
Si substrate
Si
Al mask
Acc.V Spot Magn Det WD Exp
100 µm
15.0 kV 3.0 198x SE 10.2 4 ASIMP Al Wafer 0.5hr 07/00 Xu
(b)
Al mask
Si sidewall
Si substrate
Acc.V Spot Magn Det WD Exp
20 µm
15.0 kV 3.0 1581x SE 10.1 4 ASIMP Al Wafer 0.5hr 07/00 Xu

Figure. 5-19. **Standard DRIE etch process on a 4-inch Al-mask wafer.**
(a) 0.5 hr DRIE anisotropic etch of Si.
(b) Zoom in view of (a)

First, the effect of a 30 min Si anisotropic etch, corresponding to a 45 μm depth, is examined. The SEM of the etched 4-inch Al mask wafer is shown in Figure 5-19. There is no significant difference between the Al-mask wafer and the PR-mask wafer within the 30 min process time, except for a slight roughness on the bottom of the substrate, as in Figure 5-19(b). However, for a long time etch (greater than 2.5 hr), hillocks, which are associated with the micromasking effect, generate on the bottom surface, as in Figure 5-20.

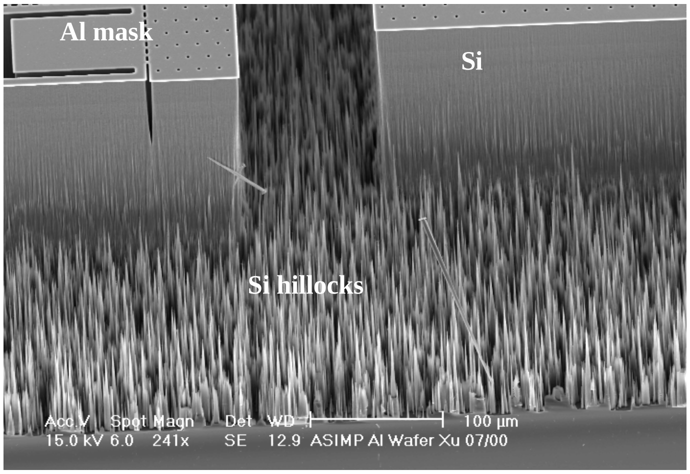

Al mask
Si
Si hillocks
Acc.V Spot Magn Det WD 100 µm
15.0 kV 6.0 241x SE 12.9 ASIMP Al Wafer Xu 07/00

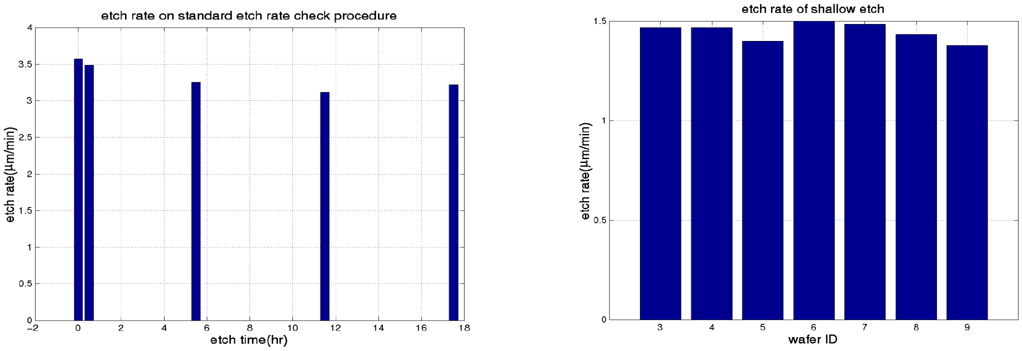
Figure. 5-20. Silicon hillocks generated on the bottom surface.

Second, the long-term effect of etching Al-mask wafers in a ICP chamber is investigated. Seven Al-mask wafer runs, adding up to 17.5 hr total etch time (equivalent to 35 normal runs), emulated the long-term effects on the processing chamber. Etch rate monitor wafers were inserted in runs between each test wafer and there was a 1 hr chamber condition etch, before each monitor wafer. The etch results are compared with the original record when the machine was installed. The etch time on the monitor wafer is 3 min, only pure SF_6 gas is fed into the chamber, and the vertical etch rate of the average over five-point measurements on the wafer, is 3 µm/min to 3.33 µm/min.

Table 5-4: 3 min Etch in the ICP Chamber with Pure SF_6

Parameters	Parameter Settings
SF_6 (sccm)	130
O2 (sccm)	0
Coil power (W)	800
Platen power (W)	3
Pressure (mTorr)[a]	25
APC angle (%)	72

[a] APC angle is fixed and pressure is measured.

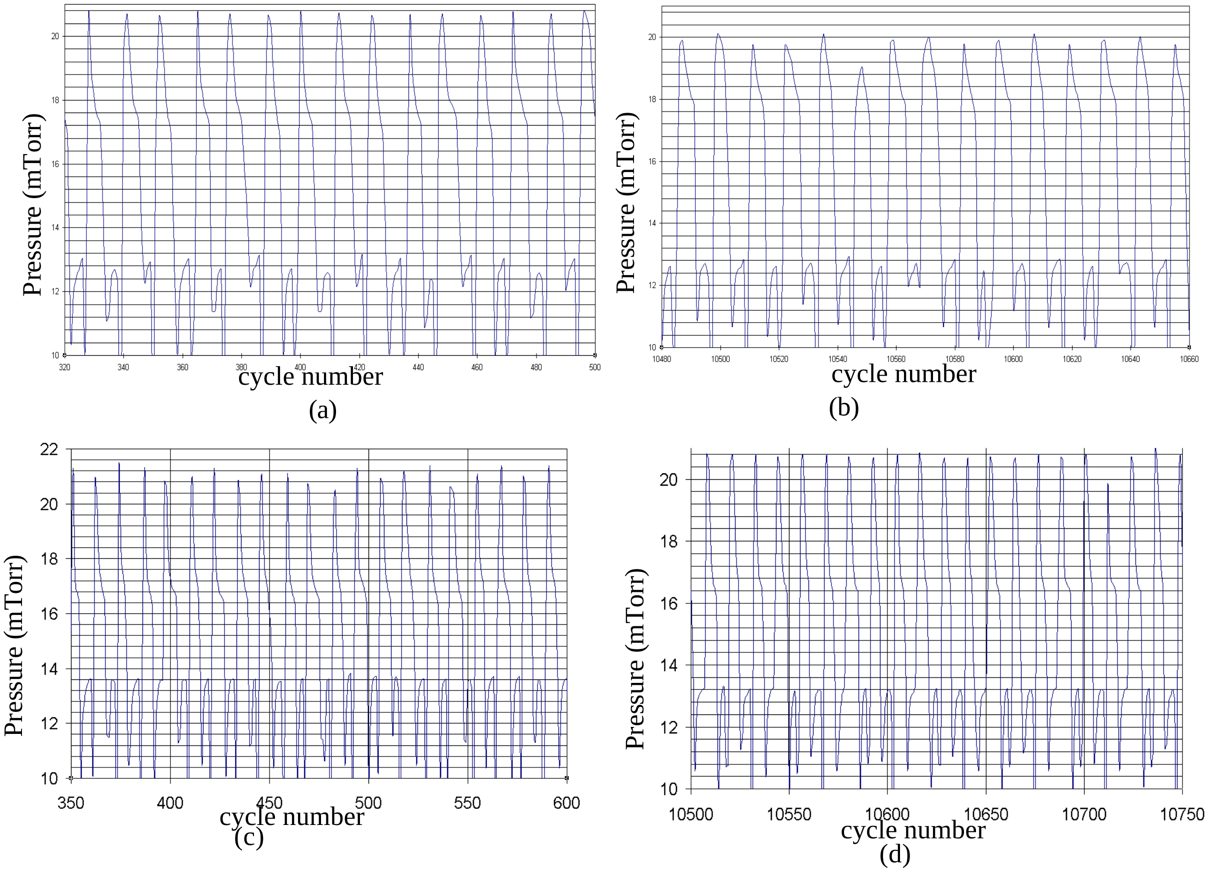


(a) (b)

Figure. 5-21. Long-term Si DRIE results for a 4-inch wafer with an Al mask.
(a) Monitor wafer etch rate.
(b) Standard recipe's etch rate.

Figure 5-21(a) shows the data of etching monitor wafers and Figure 5-21(b) show the data of DRIE etch rates on the Al-mask wafers with trench patterns. There is no apparent indication of system performance degrading within the equivalent 35 Al-mask wafer runs. The DRIE etch rates on PR-mask wafers are 1.53 μm/min before the experiment and 1.36 μm/min after the experiment. The first and last Al mask wafers have etch rates of 1.47 μm/min and 1.38 μm/min respectively. Etch rates of the monitor wafers are 3.57μm/min before and 3.22 μm/min after. This variation is within the system performance specification when the tool was installed and qualified.

Another parameter reflecting the STS ICP system status is the chamber pressure during the processing. Based on the experience from the equipment manufacturer and ourselves, the deviation of the chamber pressure from the nominal value indicates a change of the chamber condition, and therefore of the etching. The chamber pressure during the DRIE process was monitored, as shown in Figure 5-22. The chamber pressure during etching cycles of Al-mask wafers is about 2 mTorr lower than PR-mask wafers. The



(a)

(b)

(c)

(d)

Figure. 5-22. Monitoring of chamber pressure over 3 hr etch on the Al mask wafer and photo resist mask wafer.
(a) At the beginning of the Al mask wafer etch.
(b) At the end of Al mask wafer etch.
(c) At the beginning of photoresist mask wafer etch.
(d) At the end of photoresist mask wafer etch.

plasma disassociates reactive gases, polymers on the chamber sidewall, and PR into gas phase C-F radicals, accounting for the chamber pressure increase. Whereas, with the Al mask, not only the C-F radical source from the PR-mask has been eliminated, but also the polymer coated on the chamber sidewall is depleted by the plasma without C-F radical redeposition. Therefore, the chamber condition and radicals in the plasma environment are affected. Usually, attention should be paid to the decrease of chamber pressure and the logging data should be compared with the status when the machine was installed. Frequent running of the chamber condition process is required in order to generate consist etching results.

The measured etch rate of Al mask material under the standard process recipe in the DRIE system is between 16~38 Å/hr. Overall, we believed that for a short 30 min ICP Si deep trench etch required in the post-CMOS micromachining process, the micromasking effect is not significant. With cautious procedure and frequently chamber cleaning and conditioning, the wafer level process can be conducted in the STS ICP system with consistent results. However, for other types of applications which require long etch with metal mask, it is not recommended to expose the mask layer directly in the ICP RIE system.

5. 4. 4 A Modified Process

As discussed above, at the wafer level, the dielectric etch imposes the most processing difficulty. The etch rate of the dielectric in RIE is significantly reduced when large areas of metal are exposed to the plasma. The short term effect of micromasking on the etching of the wafer and the long term effect on the chamber status are a potential disadvantage for the high volume production. Therefore, a post-CMOS micromachining process which can reduce the metal exposure to the plasma environment, but still keep the simplicity of the process is required.

A modified process flow for wafer-level fabrication with an integrated wafer dicing scheme is proposed in Figure 5-23. A PR-mask is used in the dielectric etch to reduce the exposed metal area. When the continuous metal mask area is less than 2 mm on either side, the micromasking effects are not significant in the oxide etch, as in Figure 5-15. Most MEMS devices are smaller than 1 mm^2, and wafer dicing usually requires 200 μm to

500 μm spacing. This PR-mask layer is made by first concatenating all the metal (Al for most foundry service we chose) layers in the design into a new pseudo layer, then shrinking this pseudo layer by 3 μm. Therefore, only the MEMS structures are exposed to the etch, achieving the same accuracy and resolution of critical dimensions as in the CMOS foundry, while the remaining area, *e.g.* circuit and bonding pads, is covered by the PR mask. The alignment of the PR mask and the CMOS wafer can be easily achieved within the shrink dimension.

After the CMOS wafer returns from the foundry, Figure 5-23(a), a 8 μm thick hard-baked photoresist layer is applied and patterned, Figure 5-23(b), followed by a SiO_2 etch, with reduced-O_2 concentration in the plasma, to open etch pits to the Si substrate through dielectric layers, Figure 5-23(c) and Figure 5-24. The SiO_2 etch rate is only reduced by 20%, compared to the previous work [60]. Without a PR mask, the etch rate is reduced by 65%. The CMOS wafer is then attached to a carrier wafer by a double-stick dicing tape, and a thick PR layer is coated. Stacking a CMOS wafer on a carrier wafer by a dicing tape increases the surface temperature of the etched wafer by less than 5.5°C during the Si etch, and the process with stacked wafers generates same results as those of the single wafer. This CMOS wafer is partially diced to 50 μm above the wafer bottom, as Figure 5-23(d). After all the PR layers are removed, the wafer goes through a deep Si trench etch (Figure 5-23(e)) and a Si isotropic etch (Figure 5-23(f)), as in [91]. No micromasking is observed in this Si-etch release step, Figure 5-24. The deep Si trench etch does not adversely affect the DRIE system assuming careful choice of process parameters, limited processing time and Ar/O_2 plasma cleaning of the chamber after the etch. Finally, the

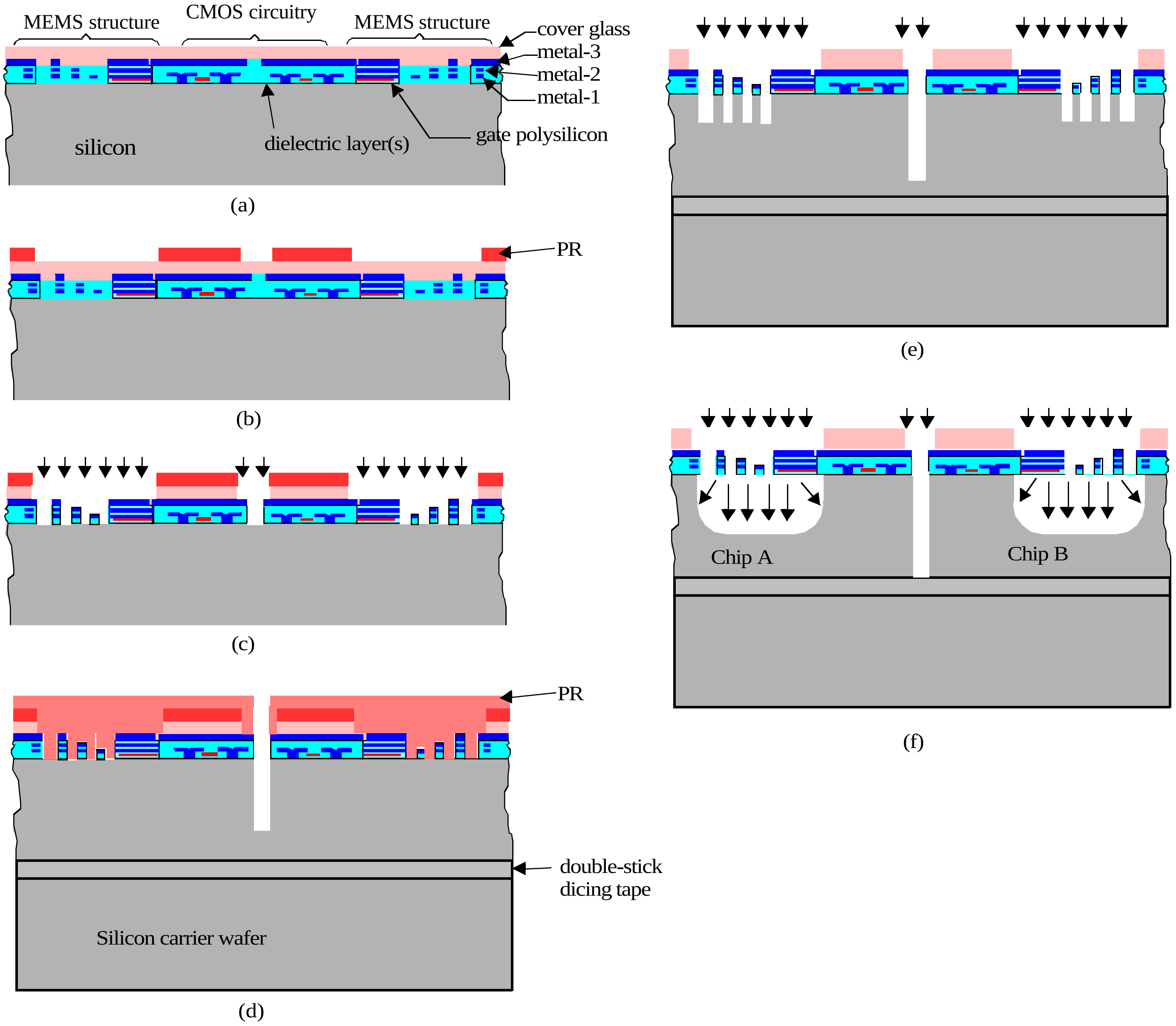

MEMS structure
CMOS circuitry
MEMS structure
cover glass
metal-3
metal-2
metal-1
silicon
dielectric layer(s)
gate polysilicon
(a)
PR
(b)
(c)
PR
double-stick
dicing tape
Silicon carrier wafer
(d)
(e)
Chip A
Chip B
(f)

Figure. 5-23. **The post-CMOS micromachining process flow at the full wafer level.**
(a) Wafer from CMOS foundry service.
(b) Wafer with spin-coated and patterned PR.
(c) Wafer after the anisotropic etch of dielectric layers.
(d) Stacking the CMOS wafer on another carrier wafer by double-stick dicing tape, followed by spin-coating another layer of PR. Then the device wafer is partially diced.
(e) After removing the PR, the entire stack of wafers goes through an anisotropic deep Si trench etch.
(f) The final Si isotropic step releases MEMS structures. Metal layer (*e.g.* metal-1, metal-2 and metal-3) combinations yields various structure heights. The chips are separated by this etch step at the same time.

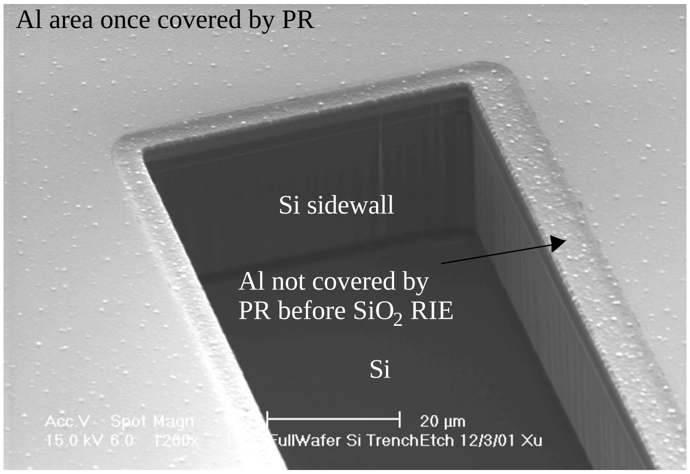

Al area once covered by PR
Si sidewall
Al not covered by PR before SiO_2 RIE
Si
Acc.V Spot Magn
15.0 kV 6.0 1200x
20 µm
FullWafer Si TrenchEtch 12/3/01 Xu

Figure. 5-24. **A Si wafer is etched in STS for 30 min with Al as an etch-resist mask. No surface roughness, induced by the micromasking effect, is observed.**

chips, which are separated by Si etch steps (Figure 5-25), are ready for packaging.

Without sacrificing the resolution of MEMS structures and increasing the complexity of the process, this proposed process flow solves the micromasking problem in the dielectric etch. The leftover cover-glass functions as a mask layer to prevent the exposure of large metal area in the DRIE Si anisotropic etch and isotropic etch. Therefore, concerns on the potential effects on ICP chamber due to high volume production with metal mask are also alleviated.

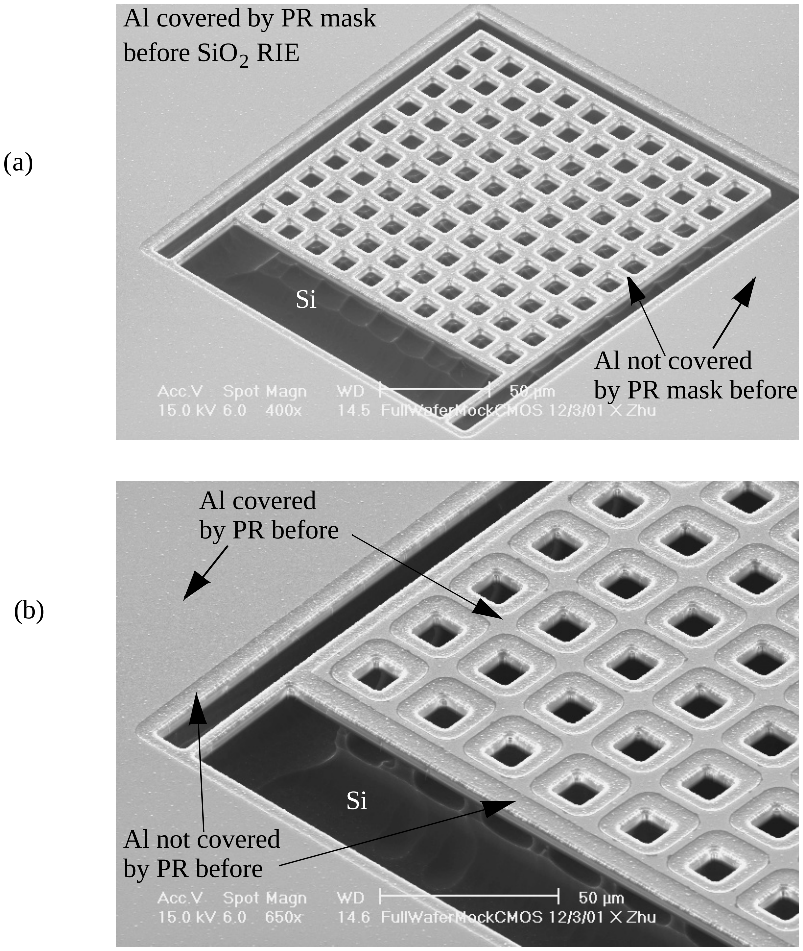

(a)
Al covered by PR mask before SiO_2 RIE
Si
Al not covered by PR mask before
Acc.V Spot Magn WD 50 µm
15.0 kV 6.0 400x 14.5 FullWaferMockCMOS 12/3/01 X Zhu
(b)
Al covered by PR before
Si
Al not covered by PR before
Acc.V Spot Magn WD 50 µm
15.0 kV 6.0 650x 14.6 FullWaferMockCMOS 12/3/01 X Zhu

Figure. 5-25. **A test microstructure resulting from the entire process flow. The substrate in the etch-pit area is smooth (a), and the microstructure surface is clean (b). The micromasking effect is negligible during the full wafer scale post-CMOS process.**

6

Applications of Post-CMOS Micromachining

6. 1 INTRODUCTION

There is a broad spectrum of applications for post-CMOS micromachining technology. These include inertial sensors, acoustic devices, infrared sensors, optical switches, RF components, and data storage devices, *etc.* The unique characteristic of post-CMOS micromachining determines advantages of this approach over other fabrication methods. In this chapter, two applications of post-CMOS micromachining will be discussed to illustrate the benefits of fabricating MEMS devices directly on CMOS chips. They are RF MEMS passive components and bulk micromachined accelerometers.

6. 2 MEMS INDUCTORS

The ever increasing competition in the wireless communication market continues to provide the incentive for low-cost RF systems. Integration of on-chip inductors is one of the key efforts in this area. On-chip inductor research includes optimization of modeling and layout [95][96][97], and process technology enhancements to improve performance [98]. Previous work related to inductor performance optimization have focused on layout and design improvements. Performance improvements through different technologies have also been explored [98][99][100][101]. In this section, the loss mechanism of on-chip inductors is first briefly summarized. Then an electromagnetic (EM) simulation is adopted to evaluate the performance improvement by different technologies. Last are on-chip inductor performance improvement by post-CMOS micromachining is demonstrated and measurement results are compared with the simulation data.

6. 2. 1 Loss Mechanism of an On-chip Inductor

Inductors are intended to store all electromagnetic energy. However, there is a loss of energy during each cycle of operation. As summarized in Figure 6-1, besides the finite coil resistance loss, the losses in the substrate contribute to energy losses and hence reduce the quality factor (Q), which is defined as:

$$Q = \omega \frac{energy\ \ stored}{average\ \ power\ \ dissipated} \tag{6.1}$$

Where ω is the operation frequency. Currents flow through capacitance between the inductor coil and substrate, or in the other words, the EM field couples into the substrate through the dielectric between the coil and substrate. These currents cause I^2R ohmic losses in the substrates. Also, the alternating EM field radiating from the inductor generates eddy currents in the substrate which produce another EM field that opposes the original field. This phenomenon adds another loss mechanism for on-chip inductors.

Layout optimization only improves the quality factor at specific frequencies, or at a specific frequency. However, layout changes alone do not reduce the major loss mechanism of the on-chip inductors at high frequency, the substrate loss, and the improvement is

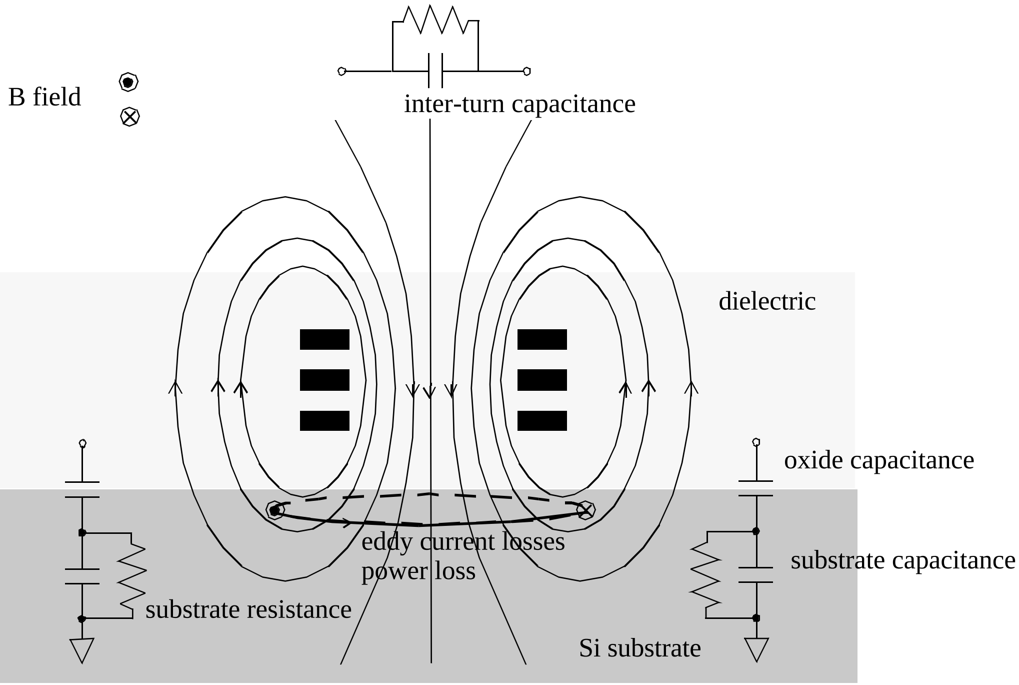

B field
inter-turn capacitance
dielectric
oxide capacitance
eddy current losses
power loss
substrate capacitance
substrate resistance
Si substrate

Figure. 6-1. Summary of different type of losses for a on-chip inductor.

limited. Figure 6-1 suggests that, in order to improve the quality factor of inductors at frequency above 2 GHz, losses in substrate must be eliminated by either shorting the substrate or making it open, and the wire resistance of inductors needs to be reduced as much as possible.

A common practice for the RF circuit designer is to put a ground plane underneath the inductor to minimize the loss in the substrate. The solid ground shield helps to reduce the substrate resistance, but it also induces opposing flowing loop currents due to Lenz’s law. These currents produce a negative mutual coupling that reduces the magnetic field and decreases the overall inductance. One approach suggested by Yue and Wong [102] is the use of patterned ground shields that reduces the induced loop current by insertion of slots in the shield. The main drawback of this technique is that the parasitic capacitance to substrate is significantly increased. Patterned ground shields are effective for lower frequency applications where the parasitic capacitance can be absorbed in the LC tank.

Other approaches useful for reducing substrate losses include increasing the space between the inductor and substrate, increasing the substrate resistance or eliminating the substrate under the inductor. The high resistivity silicon [95] or sapphire substrates has been demonstrated to fabricate high Q planar inductors, achieving quality factors of 40 at 5.8 GHz for an 1.4nH inductor [98]. However, the use of high resistivity material is not common in a CMOS process due to processing difficulties and many sub-micron CMOS technologies use epitaxial silicon wafers. Chang *et al.* proposed elimination of substrate losses of inductors by removing the underlying silicon using front side etch of silicon, by wet etching [28] or by gaseous dry etching [100]. These techniques have inherent limitations that the distance of transistors from the inductor is determined by the dimensions of the inductor and the time of the etch. This distance introduces ohmic losses in the interconnect resistance. Other approaches to eliminate silicon from below the inductor have used back side wet etching techniques [99]. Another approach to reduce substrate loss is by increasing the space between the inductor and substrate, *e.g.* using polyimide as a spacer [103][104].

6. 2. 2 FEM Simulation to Evaluate Different Processing Technology[1]

As mentioned above, most published results demonstrate data by introducing a particular type of technique upon the renovation of the existing fabrication process, such as increasing the coil thickness or creating a large separation between the inductor and the substrate. However, the potential capabilities to enhance an inductor performance by these new techniques are left unevaluated. For example, there is no published results on the relationship of the Q improvement *vs.* the increase of the gap between the inductor and the substrate. And there is no published results on the relationship of the Q improvement *vs.* the increase of the spiral thickness. Therefore, there is no conclusion on which modification in fabrication is the most efficient way to improve the inductor's Q.

---

[1] This simulation work was initialized and partially completed while working with the Microelectronic SiGe group at IBM, East Fishkill, NY.

Relying on high-frequency structure simulation tools, this section investigates potential performance enhancements by scanning the entire process parameter space. Based on inductors fabricated in the IBM SiGe process, the process specification information and inductor layouts are imported into Sonnet®, a commercial Method of Moments EM field simulator [105]. The simulator was tuned to match the measurement data up to 5 to 10% accuracy without sacrificing the computation time. The parameters in the simulator needed to be justified include the meshing density and boundary conditions. By varying setups of material properties and geometric parameters of structural materials in the simulator the entire achievable range of process parameters were covered. The simulation results were used to predict the most promising avenues for improvement, and to offer a guideline for fully and economically exploiting each fabrication technique.

- **Simulation Setup**

The inductors being examined include 0.1 nH, 0.3 nH, 0.6 nH straight line inductors and 1 nH and 5 nH square spiral inductors. As in Figure 6-2(a), the spiral inductor consists of a top metal layer as the spiral and a 2.3 μm thick copper layer as the return path, while the straight line inductor only consists of the top metal layer, as in Figure 6-2(b). In most cases, the top metal layer is made of 4 μm aluminum, except for the thick spiral layer simulation which uses copper. Spiral inductors of other shapes, *e.g.* octagonal, are not included in this work due to the exponential increase of simulation time, and they are not expected to provide additional insight. The substrate is 700 μm thick silicon. It is separated from the inductor by the dielectric material, which is usually 12 μm thick silicon dioxide as in the SiGe process specifications. Between the spiral and the return path is a

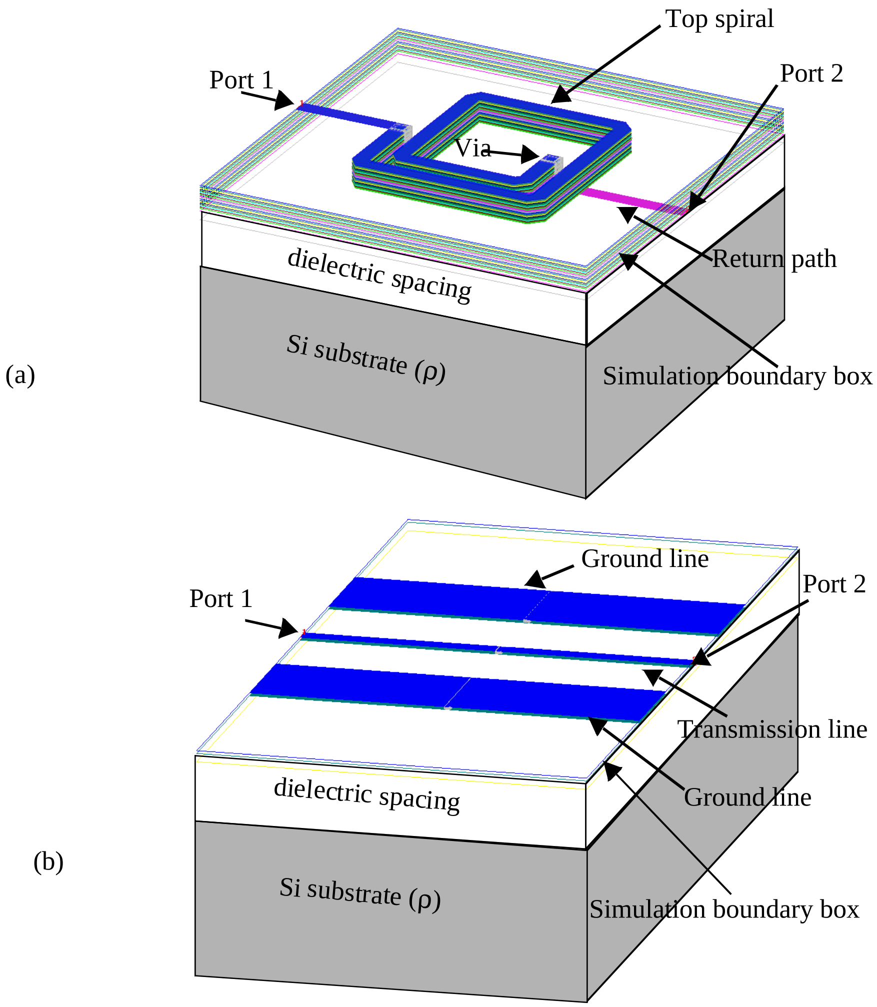

Top spiral
Port 1
Port 2
Via
Return path
dielectric spacing
Si substrate (ρ)
Simulation boundary box
(a)
Ground line
Port 1
Port 2
Transmission line
Ground line
dielectric spacing
Si substrate (ρ)
Simulation boundary box
(b)

Figure. 6-2. Typical inductor designs in the simulation (the substrate is not shown in the figures).
(a) A spiral inductor design.
(b) A straight line inductor design.

4 μm thick oxide layer. All the oxide layers have dielectric constants equal to 4.1.

In the device fabrication, the wafer resistivity varies from 0.1 Ω·cm to 1000 Ω·cm. The metal thickness used in the spiral inductors ranges from 2 μm to 34 μm. In the front-end-of-line (FEOL) process flow, the engraved substrate is filled with polyimide (loss tangent around 0.001) as a base for inductors. Alternatively, the post-CMOS micromachining technology can create free standing inductors above the substrate. These fabrication variations can be represented in the simulation by changing parameters of metal and dielectric layers in the simulation setup. Nominal values of metal layer sheet resistance, wafer resistivity, dielectric constant and dielectric loss are used in the simulations. Book values are adopted for the metal conductance to calculate the skin effect [106]. The thick metal layers are approximated in simulation by paralleling multiple infinitely thin conducting layers, with a metal track height to metal track width aspect ratio of less than 1:5, as suggested in the Sonnet manual [105]. Adjustments of meshing, cornering and boundary conditions in the simulation are required to ensure the simulation accuracy from an 100 MHz to 50 GHz frequency range [107]. Two-port inductor layouts are imported into the simulator through GDSII format. The Q definition follows the single-end Q configuration, in order to be comparable with previous data [95]:

$$Q(f) = -\frac{Im\{Y_{11}\}}{Re\{Y_{11}\}} \tag{6.2}$$

Simulation results of typical spiral inductor designs, *e.g.* an 1 nH and 5 nH spiral inductor with 25 μm wide spiral and 45 μm wide pitch and a 0.6 nH straight line inductor, match the measurements up to 3%, as shown in Figure 6-3.

- **Simulation Results and Discussions**

Figure 6-4 shows the simulation results of the peak inductor Q *vs*. the wafer resistivity. For a spiral inductor design, higher wafer resistivity yields higher Q. However, even 1000 Ω·cm substrates cannot yield the maximum achievable Q (defined as the inductor standing in the air). Increasing substrate resistivity for spiral inductors from 10 Ω·cm to 1000 Ω·cm provides a maximum increase in Q of 50%, which is similar to the previous

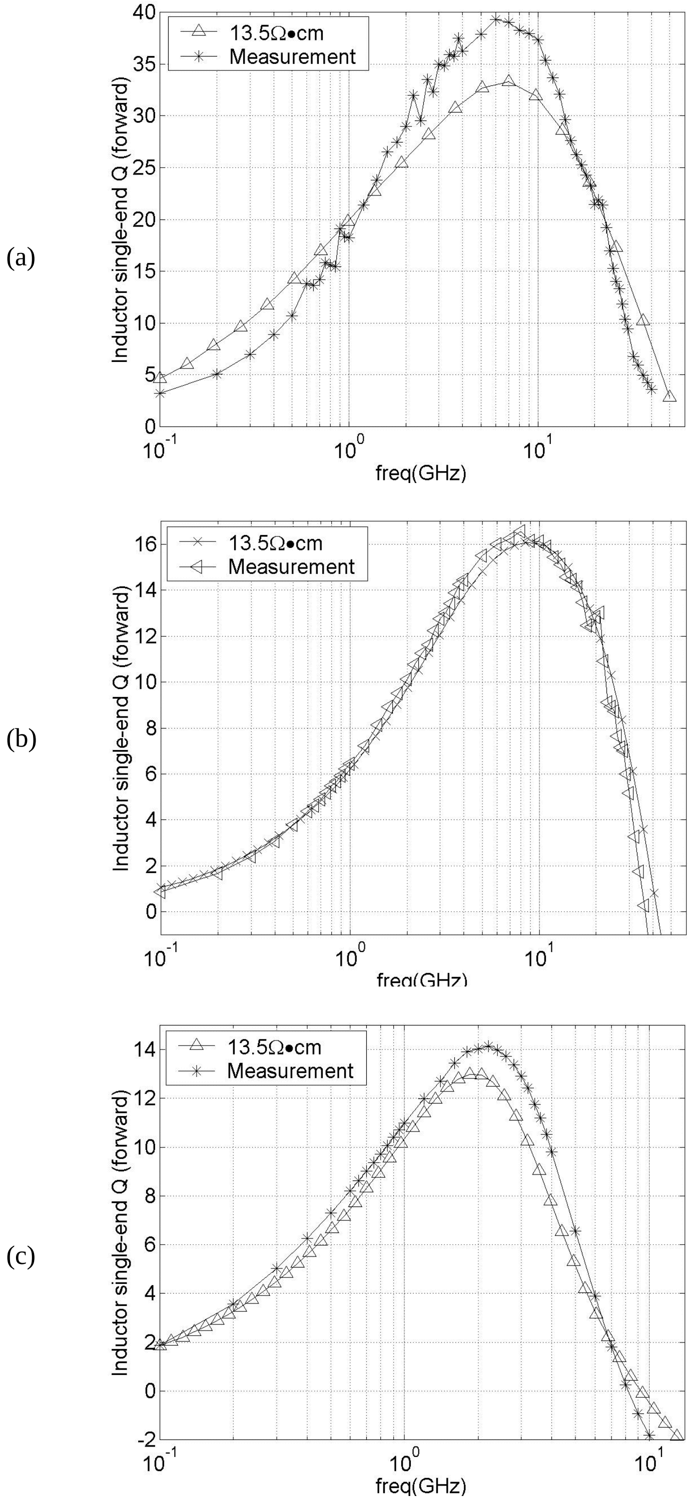


Figure. 6-3. **Typical simulation results and measurement data of on-chip inductors (1nH) with wafer resistivity of 13.5 *W* • cm.**
(a) 0.6 nH straight line inductor.
(b) 1 nH spiral inductor.
(c) 5 nH spiral inductor.

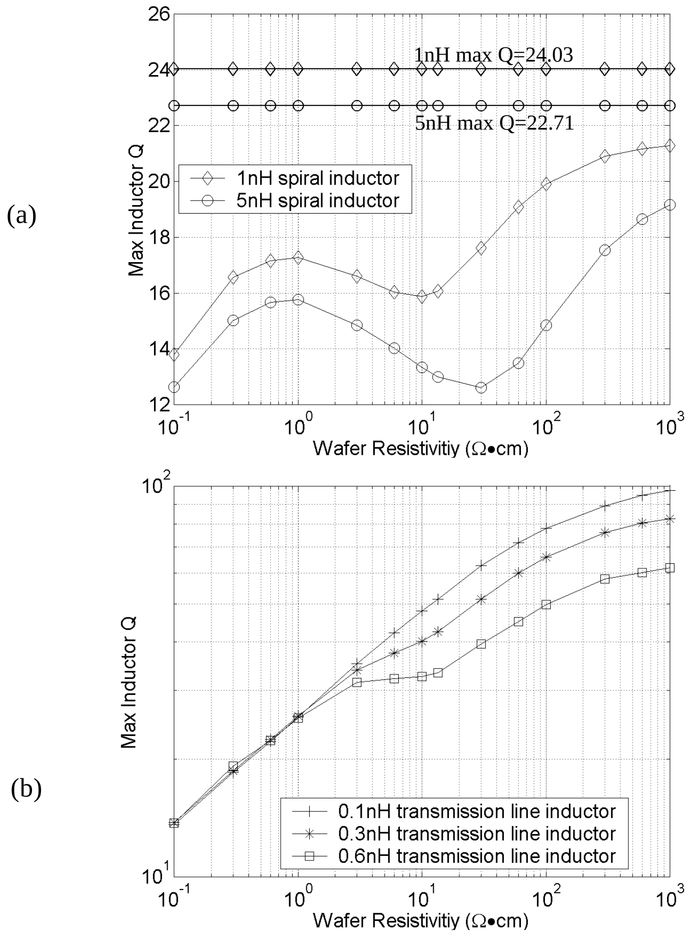


Figure. 6-4. **Maximum inductor Q *vs.* wafer resistivity.**
(a) Spiral inductor designs.
(b) Straight line inductor designs.

data by Burghartz [98]. The Q of spiral inductors has a local maximum with wafer resistivity value around 1 Ω·cm. A larger spiral inductor has a longer substrate loss path, therefore its Q has larger improvement than that of a small inductor, due to the increased substrate resistivity. This effect is much less significant in straight-line inductors, where the EM field pattern surrounds the straight-line inductor and is perpendicular to the substrate. The EM field of straight-line inductors penetrates much more deeply into the substrate than the field of spiral inductors, resulting in a longer loss path and larger loss.

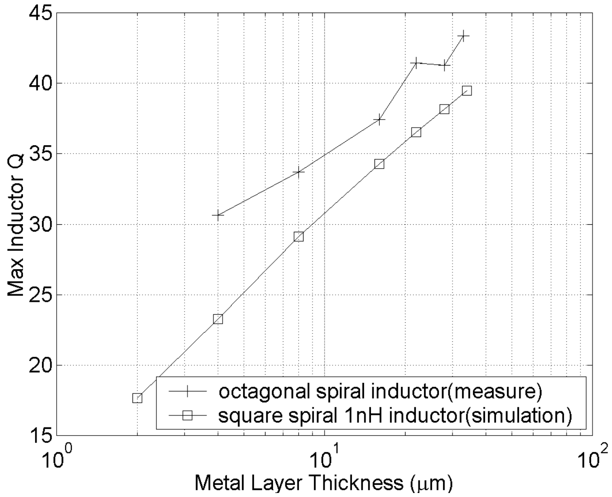


Figure. 6-5. Maximum spiral inductor Q *vs.* metal thickness.

Figure 6-5 shows the measured and simulated results for Q *vs.* the metal thickness. The measurement data are from octagonal designs while the simulation uses square spirals due to the memory and simulation time constraints. The Q increases linearly with the logarithm increase of metal thickness. This indicates that thickening the metal reaches a point of diminishing returns for improvement in Q. Several reasons account for this eventual saturation of Q with increasing metal thickness:

- The wire resistance change as the inverse of metal thickness (1/t) at high frequencies due to skin effects. Figure 6-6(a) plots the Q at 1 GHz as a function of metal thickness. For comparison, the simulated and measured resistances of 2 μm thick spiral are extrapolated using a 1/t dependence. The difference between the curves illustrates the impact of the skin effect on resistance.
- With the pattern of EM field generated by the coil [108][109], the current crowding effect steers the current to only one side of the metal trace. Usually, the current flows on the outer sidewalls for the outer turn, swings to the inner sidewalls as the

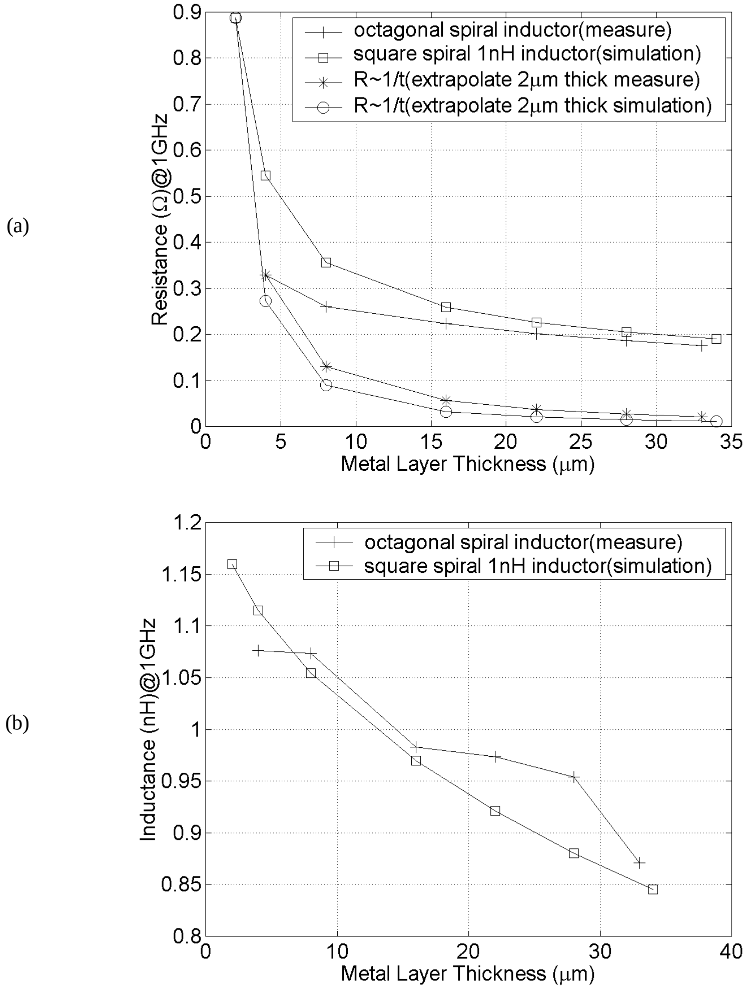


Figure. 6-6. **Simulated and measured spiral inductor resistivity (a) and inductance (b) vs. metal layer thickness at 1 GHz. In the simulation, the square shape is used to approximate the octagonal design.**

metal trace spiraling inward, and flows on the inner sidewall for the inner turn. The switching from outer surface to inner surface is due to the pattern of the magnetic field.

- For the identical layouts, the inductance drops as the thickness increases, as illustrated in Figure 6-6(b). This drop is due to a decrease of the effective spiral radius due to the aforementioned current crowding effects.
- The substrate affects the current distribution, as illustrated in Figure 6-7. At high

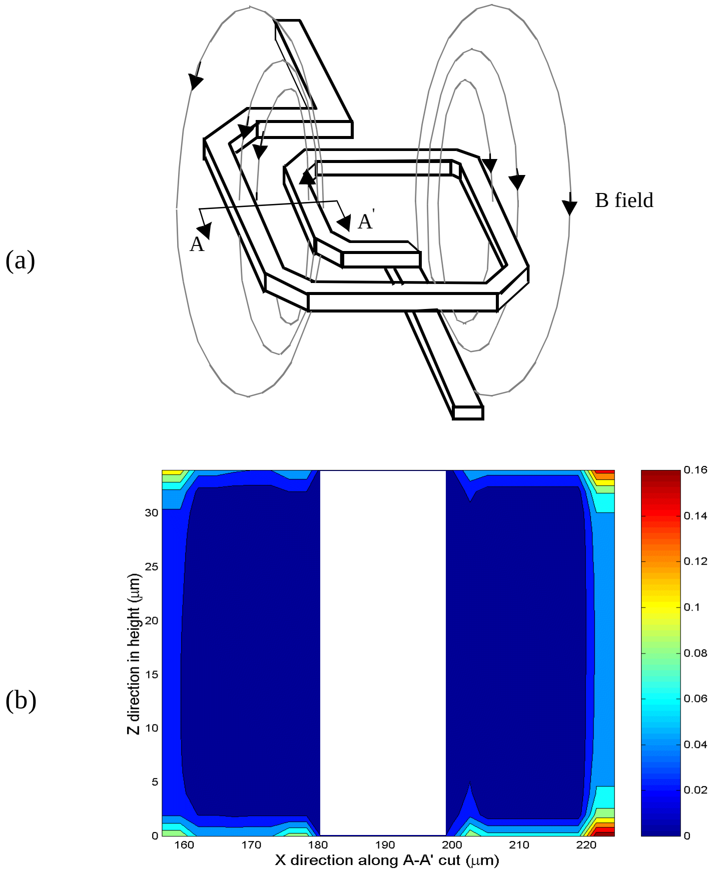


Figure. 6-7. **Simulation of thick metal spiral inductor.**
(a) A thick metal spiral inductor simulated in Sonnet.
(b) The current density distribution at the cross section of A-A' in (a). The current flow switches from the left side to the right side due to the B-field pattern (a). The color bar illustrates the relative current flow density.

frequency, more current flows at the bottom surface of the metal traces due to the capacitance coupling effect.

- Most important, the current density distribution is not uniform along and across the spiral wires, and it concentrates on the corners of the conducting wires. The fixed resistance of the return path becomes comparable with the spiral resistance and starts to dominate total series resistance, and also contributes to the slowing down of Q improvement with increasing metal thickness.

In order to reduce substrate loss induced Q degradation, several techniques are used to

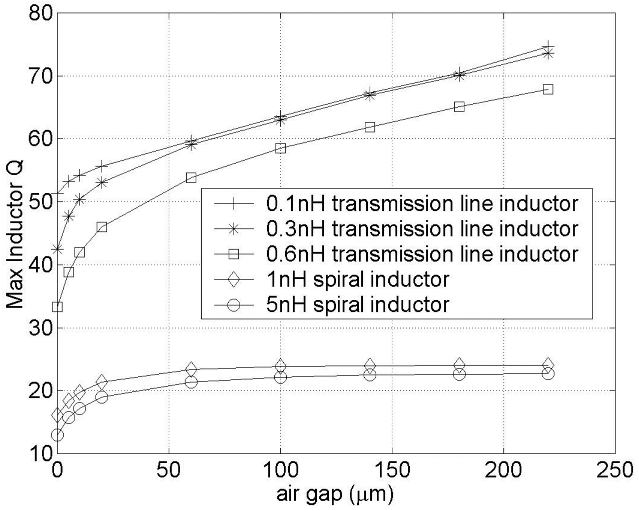


Figure. 6-8. **Maximum inductor Q *vs.* air gap depth.**

remove the substrate underneath the inductor. These include removal of the substrate from the backside by wet etch [99], or from the front side by wet etch [28] or vapor phase etch [100] and RIE dry etch [101]. In the simulation, an air dielectric layer is inserted above the silicon substrate to emulate this removal of part of the substrate. The technique of backside Si removal is treated as an infinite air gap in the simulation. It is clear from Figure 6-8 that substrate removal effectively improves the Q, and the Q value reaches the maximum at the 100 μm air gap for a 400 μm inductor outer diameter (O.D.). This indicates that the EM field extends to about 100 μm range below this size of spiral inductor. Extra etching into the substrate reduces the mechanical strength of the chip and does not improve performance. Larger inductors benefit more from substrate removal. With an inductance value of 5 nH, the Q value increase is around 200%. This matches the previous data mentioned above [101].

A dielectric layer is inserted above the Si substrate in the simulation setup with dielec-

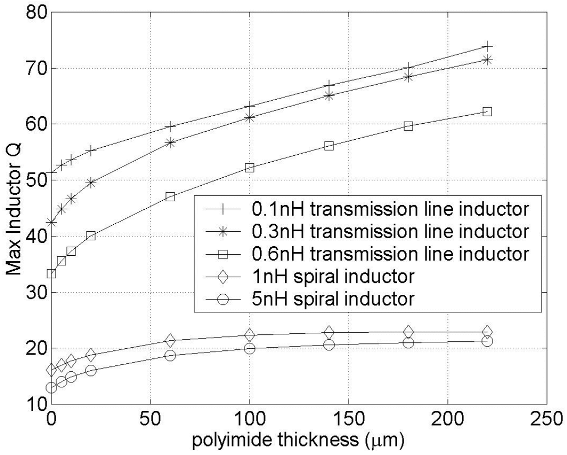


Figure. 6-9. **Maximum inductor Q *vs.* thickness of polyimide.**

tric constant(ε_r) 3.4 and loss tangent 0.001 (Dupont PI5878) to act as a thick dielectric material layer in the processing which separates the inductor and the substrate, *e.g.* SiO_2 and polyimide [103]. This material has the same intended function as the air gap dielectric. It is expected that the Q values as a function of polyimide thickness should behave similarly to those plotted in Figure 6-8. However, as shown in Figure 6-9, the Q for polyimide will reach a maximum later than an air dielectric, because the air has the lowest dielectric constant. Slight reduction of maximum Q value in this case is due to larger capacitive coupling from one portion of the spiral to another. Again, the Q improvement matches the previous data by Laney [103].

It is noticed that Q curves of straight-line designs have not become flat with 200 μm thick dielectric, compared with that of spiral designs. The reason is that the EM field generated by the straight line inductors penetrates much more deeply into the substrate than that for spiral designs, therefore a larger spacing between the inductor and the substrate is required.

Increasing the oxide thickness between inductors and the substrate reduces substrate loss is, in principle, the easiest modification of an existing process. However, due to stress issues in the wafer, the maximum thickness for chemical vapor deposition (CVD) oxide is limited to around 10 µm, which is far below the separation requirement, 100 µm, for maximum Q.

In summary, the Method of Moments tool can accurately simulate spiral and straight line inductors. Different fabrication techniques can be presented in the software by changing the parameter setups. The substrate coupling loss is a major loss mechanism along with wire resistance, especially in the straight line case. In addition to increasing metal thickness, any added fabrication steps in the FEOL or back-end-of-line (BEOL), which can locally increase the space between the inductors and substrates, will dramatically improve performance. For most practical spiral designs, a spacing of around 100 µm is sufficient, however larger spacing is required for straight line designs. Figure 6-10 demonstrates the simulation results of the maximum performance improvement of spiral inductors by combining substrate removal and thick metal. It is concluded that combination of these process modules will achieve the desired requirements much more efficiently.

6. 2. 3 Spiral Inductor in UMC Copper Low-K 0.18 mm CMOS Process[1]

In this section, the performance improvement of inductors fabricated in a UMC Cu interconnect low-K dielectric process by the post-CMOS micromachining technology is demonstrated [101]. Removal of the underlying Si and the inter-turn sidewall oxide helps

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[1] This work is supported by the Semiconductors Research Corporation (SRC) copper design contest.

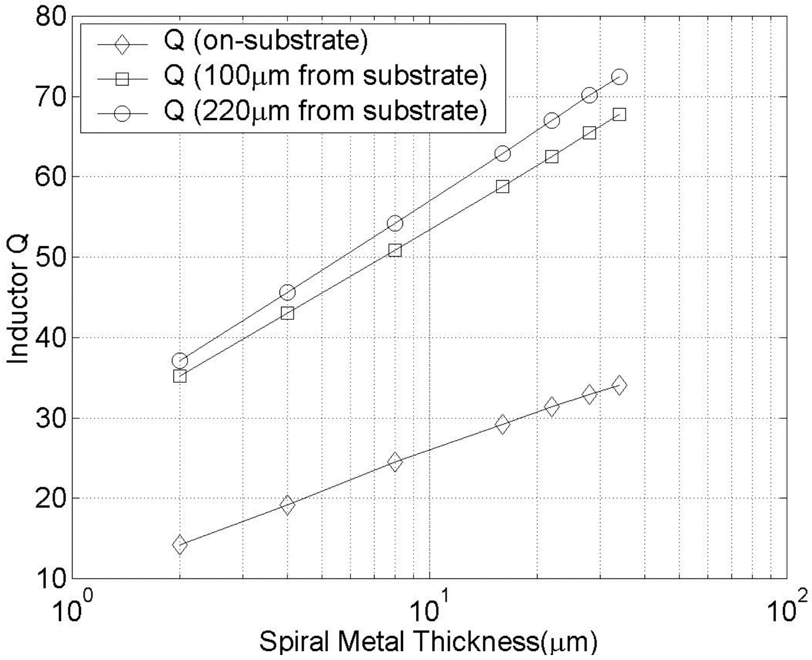


Figure. 6-10. **The performance improvement of a 1 nH spiral inductor by combining substrate removal and thick metal.**

reduce the substrate losses that dominate at higher frequencies, increase the self resonant frequency and also reduce substrate noise coupling into the inductor. This technique leverages the ever increasing number of interconnect layers used in modern processes for passive designs for lower series resistance without severe high frequency performance penalties. The processing details has been described in Chapter 5. This section covers on the process impact on circuit designs, measurement results, physical modeling to understand the performance improvement through the MEMS technology, and the mechanical structure stability for practical applications.

- **Design Consideration**

By taking the advantage of post-CMOS microfabrication, circuits can be placed about 30 μm away from the edge of the silicon etch pit and this design rule is independent of the depth of the silicon etch pit. The circuits are protected by the top metal of the CMOS process. There is a disadvantage as top metal cannot be used generally for arbitrary interconnect and is grounded. If an extra mask is used at the wafer level, as stated in Chapter 5, the top metal layers are free for arbitrary routing. The maximum width of a metal masked feature is about 30 μm due to CMP requirements in the process. The smallest width is limited to 1.5 μm due to the process constraints.

The electrical performance of the circuits is not affected by the etching steps. Inverter test structures were tested before and after the micromachining process. A 2.2 GHz single LC tank oscillator was tested to verify the operation of the transistors after the post-CMOS processing steps. The oscillator used a 3 nH single suspended inductor. The circuit consumed 10.2 mA with a supply voltage of 1.7 V.

- **Inductor Structure**

An SEM image of a suspended inductor with a single-sided connection is shown in Figure 6-11. The inductor coil is designed with four 20 μm-wide turns using the two thickest top metal layers, identified as metal-5 and metal-6 layers in the process specification. However, the metal-5 and metal-6 layers in the engineering runs were made only 0.5 μm thick. These two layers are shunted together to reduce the series resistance of the spiral. The return path consists of a shunted combination of the remaining metal layers, metal 4,3,2 and 1.

6. 2. 4 Experimental Design and Measurements

Four two-port octagonal inductors and eight one-port octagonal/square inductors, were

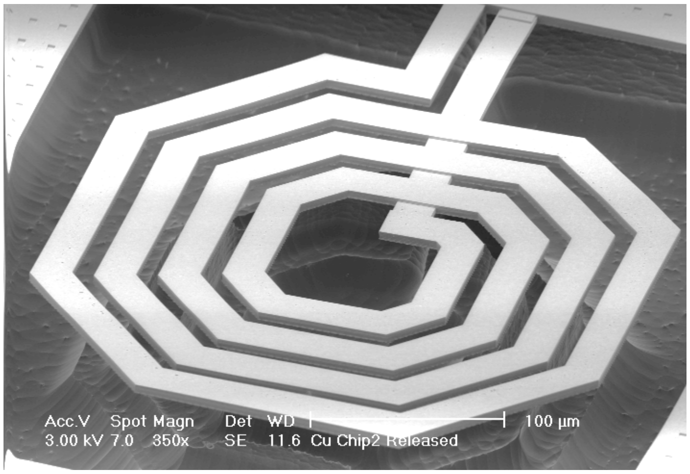


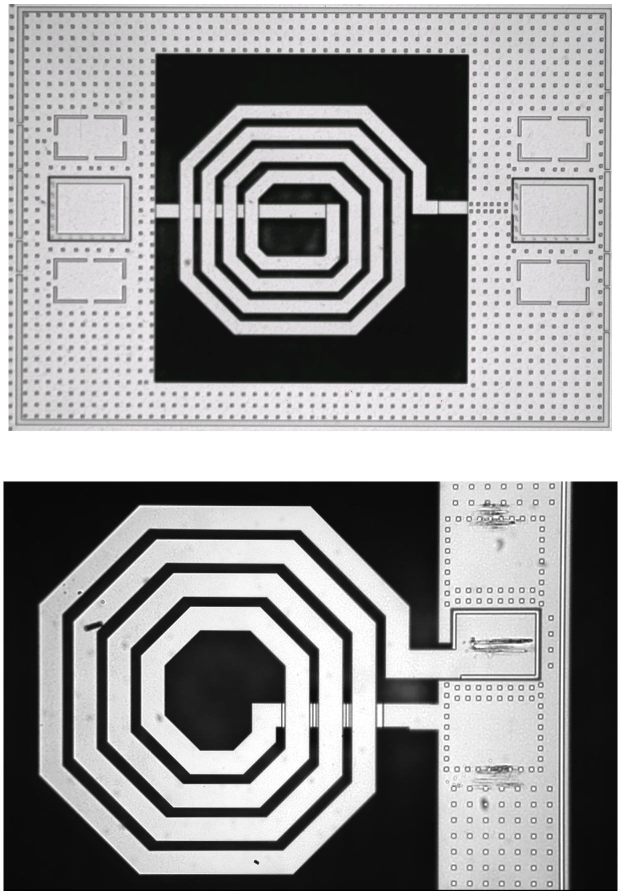
Figure. 6-11. A spiral inductor with a 100 *m*m separation from the substrate.

designed. The metal mask around each inductor is about 500 µm × 500 µm. A two port inductor and a one port inductor, along with the port probe pads, are shown in Figure 6-12(a) and (b) respectively. The surrounding mask metal has been grounded and is tied to the substrate. To investigate the effect of the micromachining on the performance improvement of the inductors, measurements were made on: unprocessed inductors, inductors after the first step of sidewall oxide removal, and inductors after the complete processing.

All inductor chips tested were from the same wafer batch and were post-processed at the same time. This set of measurements quantifies the improvement due to micromachining, including oxide removal and silicon etching.

The inductors were measured by on-chip probing using 100 µm pitch ground-signal-ground (GSG) microwave probes connected to a HP8510C network analyzer with frequencies ranging from 50 MHz to 20 GHz. Probe calibration was done using a Cascade

(a)



(b)

**Figure. 6-12. Optical microphotograph of micromachined inductor test structures showing the surrounding mask metal layer (adopted in the first UMC copper low-k process run).
(a) A double side anchored inductor along with 2-port test pads.
(b) A single side anchored inductor along with 1-port test pads.**

CS-5 calibration substrate. The probe pads were de-embedded by making measurements on dummy open and short test structures connected to test pad structures.

The performance of four two-port inductors L1-4 was compared with measurements made on three chips. The three sets of measurements were:

- Set *A* - conventional inductors without micromachining obtained from the foundry;
- Set *B* - low-K sidewall oxide was removed in areas not covered by metal;

- Set *C* - the inductors were processed as in Set *B* followed by silicon removal in all regions not covered by metal.

For eight one-port inductors, only the set A inductors and the set C inductors are compared. The two-port inductor measurement data is shown in Figure 6-13. Table 6-1 summarizes the measurement results obtained from the two-port inductors. In all calculations, port 2 is grounded. The different configurations of one-port inductors, with signal ground connected to the return path, are summarized in Table 6-2. The measurement results are illustrated in Figure 6-14 and summarized in Table 6-3.

The change in quality factor after sidewall oxide removal is not significant, however an increase of 14% to 33% in the self-resonant frequency can be seen. The reduction of the sidewall oxide capacitance is larger for the bigger inductor, causing a greater increase in self-resonant frequency. A small increase in the maximum Q was also observed due to the increase in the self-resonance frequency.

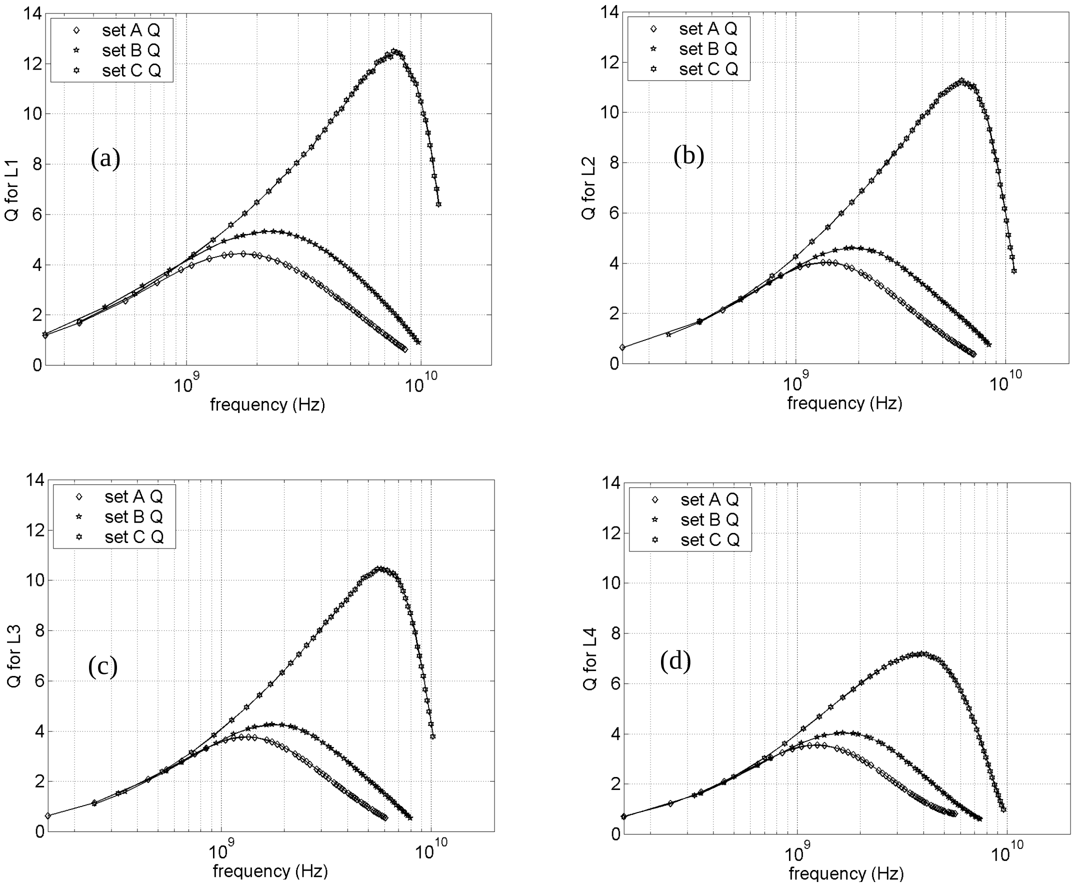


Figure. 6-13. **(a-d) Comparison of the measured quality factor of the inductors from set A (conventional), set B (oxide removal) (a) L1, (b) L2, (c) L3 and (d) L4.**

Table 6-1: **Summary of inductor measurement data from the 1st UMC run**

Property	L1			L2			L3			L4		
	set A	set B	set C	set A	set B	set C	set A	set B	set C	set A	set B	set C
L_m (nH)	3.16	3.32	3.19	3.89	3.95	3.91	4.12	4.20	4.15	4.61	4.71	4.69
Q_{max} conv.	4.39	5.32	12.5	4.02	4.60	11.2	3.76	4.25	10.46	3.64	4.09	7.61
Q_{max} f(GHz)	1.75	2.25	7.75	1.45	1.85	6.50	1.35	1.75	5.72	1.25	1.75	4.75
R_{dc} (ohms)	3.45	3.27	3.32	4.26	4.39	4.16	4.70	4.89	4.65	5.28	5.52	5.21
Outer diameter(µm)	300			336			350			365		
wire width(µm)	20			20			20			20		
# of turns	4			4			4			4		
pitch (µm)	30			30			30			30		

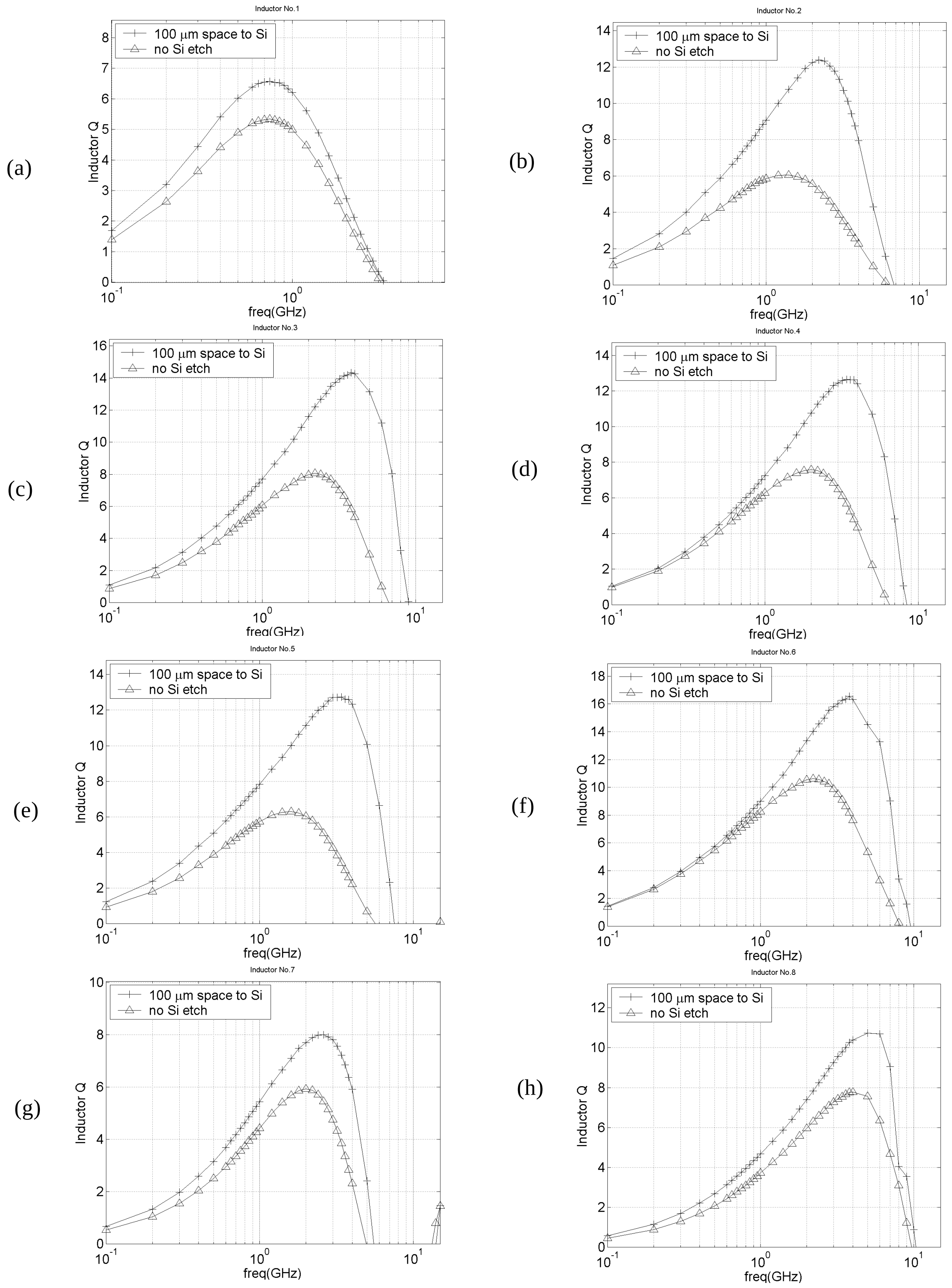


Figure. 6-14. Measurement of one-port spiral design inductors in the 2nd run from the UMC copper interconnect low-K dielectric process. The geometric description of the device is given in Table 6-2(a)Device #1 (b)Device #2 (c) Device #3 (d) Device #4 (e) Device #5 (f)Device #6 (g) Device #7 (h) Device #8.

Table 6-2: Configurations of test inductors in the 2nd UMC run

Device Number	Shape	Spiral	Return Path	Diameter (μm)	Turn	Pitch (μm)	Space (μm)	via mesh
1	octagonal	6-5-4-3	2-1	450	7	25	5	Yes
2	octagonal	6-5-4-3	2-1	420	4	38	10	Yes
3	octagonal	6-5-4	3-2-1	420	4	38	10	Yes
4	octagonal	6-5-4	3-2-1	420	4	38	10	No
5	octagonal	6-5-4	3-2-1	460	5	36	8	Yes
6	octagonal	6-5-4-3	2-1	420	4	38	10	Yes
7	octagonal	6-5	4-3-2-1	450	5	25	5	No
8	octagonal	6-5	4-3	420	4	38	10	No

Table 6-3: Summary of inductor measurement data from the 2nd UMC run

Device Number	Without Si under cut				With Si under cut			
	L_{dc}(nH)	R_{dc}(Ω)	Qmax	Freq(GHz)	L_{dc}(nH)	R_{dc}(Ω)	Qmax	Freq(GHz)
1	12.60	5.68	5.34	0.75	12.34	4.60	6.58	0.75
2	4.36	2.52	6.06	1.40	4.24	1.82	12.39	2.2
3	4.33	3.13	8.06	2.20	4.26	2.43	14.34	3.80
4	4.37	2.76	7.59	2.00	4.26	2.58	12.65	3.40
5	6.66	4.53	6.30	1.60	6.38	3.27	12.73	3.40
6	4.89	2.20	10.63	2.20	4.78	2.08	16.55	3.80
7	12.57	14.92	5.93	2.00	12.47	11.61	8.00	2.60
8	4.40	6.26	7.77	4.00	4.31	4.70	10.73	5.00

The silicon removal process step increases the maximum Q by about 100% to 180%, in either one-port or two-port configurations. For two-port inductor measurements, a smaller increase is observed in L4, the biggest inductor, due to the smaller distance of the inductor from the surrounding metal field and the fill metal. This suggests that the separation distance from the sidewall to the inductor should be large enough to minimize eddy current losses in the mask metal. The self-resonance frequency of set C increased by about 38% to 70% over set A, depending on the size of the inductor. The bigger inductors have a larger increase due to a greater reduction in capacitance to substrate (C_{ox}). The frequency at which maximum Q occurs is moved to the 5 to 8 GHz range for set C inductors from the 1 to 2 GHz range for set A inductors, an increase of 280% to 350%. Inductor L1 in set *C* achieves a maximum Q of 12.5 at 7.8 GHz, a fourteen-fold increase compared to set A. At 5.5 GHz, a five-fold improvement is seen. The one-port inductors show similar performance improvement with the substrate removed by the post-CMOS micromachining technology.

6. 2. 5 Device Modeling and Characterization

To understand the improvement due to substrate and the sidewall oxide removal, an equivalent circuit model based on physical principles is proposed. The schematic of the model for a four-turn inductor is shown in Figure 6-15. It is reported in [101] and is an extension of models proposed earlier in literature [96]. Each turn of the inductor has been modeled as a separate L-C-R segment to account for the contribution of inter-turn capacitance to the resonant frequency. Such the inter-turn capacitance has been considered insignificant in the modeling of non-micromachined inductors. The details of the model is available in [110].

The measured and modeled quality factors are compared, in Figure 6-16. The differences between measurements and model calculations of inductors in set *A* and set *B* result from a reduction in the sidewall capacitance due to the ion milling induced trapezoid cross-section of metal wires instead of rectangular shape, and a slight increase in G_{sub} due to the over-etching of the silicon during the etching of the oxide. The difference in measurements and model calculations for set *C* is due to the non-planar etch front on the sub-

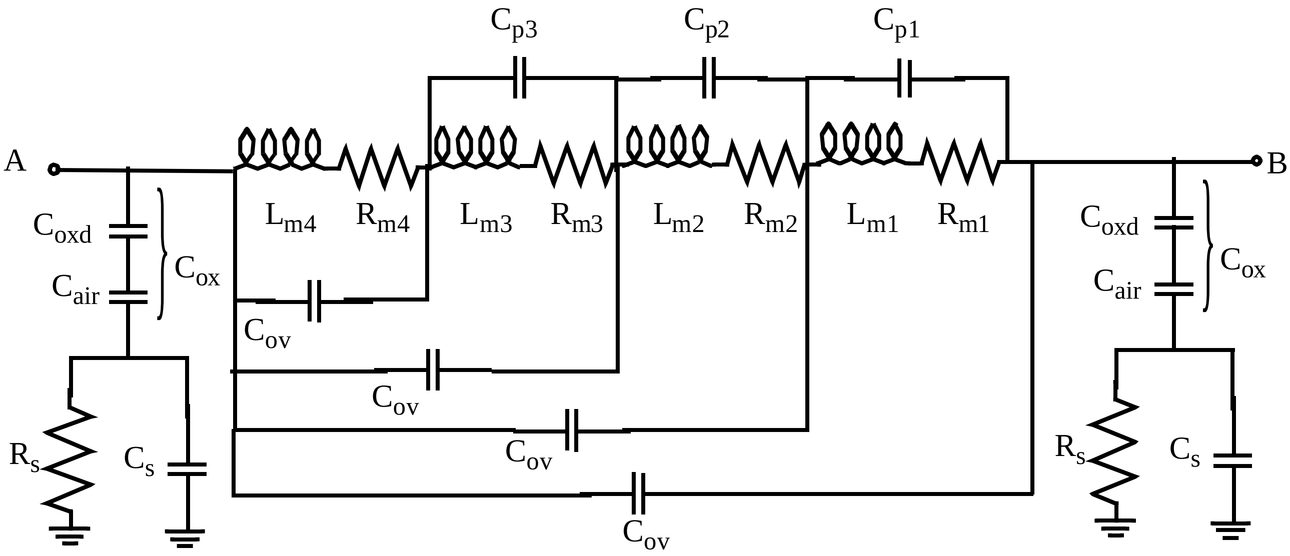
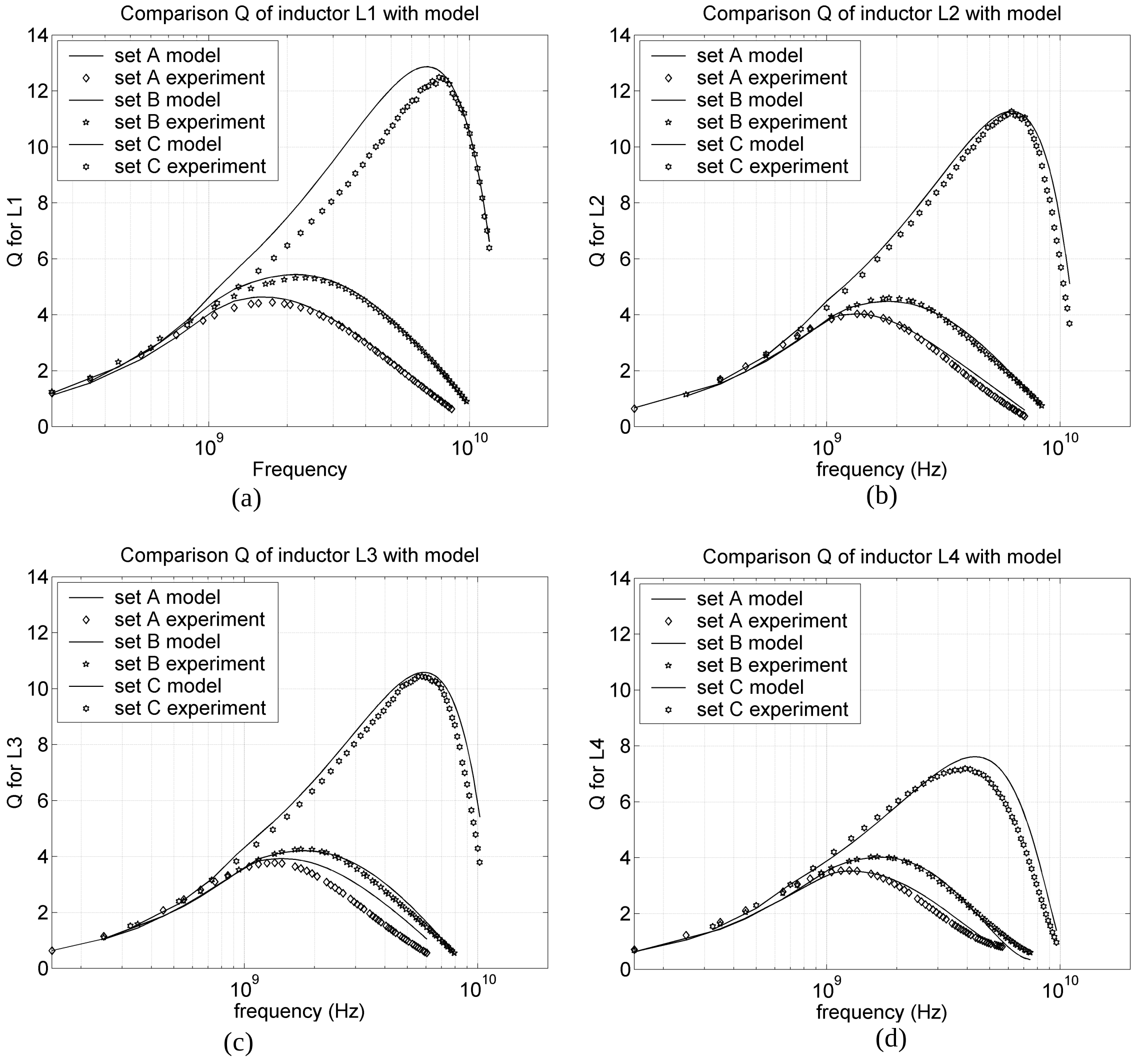


Figure. 6-15. The lumped parameter equivalent circuit for the inductor for inclusion of parasitic side-wall capacitance and substrate loss.

strate, therefor, the accuracy of effective etch depth (d_{etch}) and the substrate conductivity (G_{sub}).

This lumped model is also be used to predict the performance when the metal wires are made thicker. Figure 6-17 shows the improvement in Q by increasing metal thickness with and without micromachining for the L1 inductor. Without micromachining, the change is significant at 1 GHz, but at 5.5 GHz no improvement is gained, as substrate losses dominate the Q degradation. However, with the additional micromachining, the Q does improve at both frequencies. The improvement in Q at 5.5 GHz is lower than that at 1 GHz, as the skin depth limits the improvement of Q with increasing frequency. The quality factor of the micromachined inductor is predicted to be limited by the DC series resistance for metal thicknesses below 6 μm. Above this thickness, the inductance change with thickness must be included for best accuracy. Qualitatively, for thicker metal layers,



(a) (b) (c) (d)

Figure. 6-16. (a-d) Comparison of the measured quality factor of the inductors from set A (conventional), set B (oxide removal), set C (micromachined) with the model predictions, for inductors L1-L4.

the series resistance becomes limited by skin effects, the inter-turn capacitance increases and the self-resonance is lowered. All of these effects conspire to limit the Q. Figure 6-17 shows a similar trend as in the simulation results of Figure 6-5, where the maximum Q in the entire spectrum is plotted.

6. 2. 6 Mechanical Stability of the Suspended Inductor

One concern in design of mechanical suspended inductors is that external shocks and

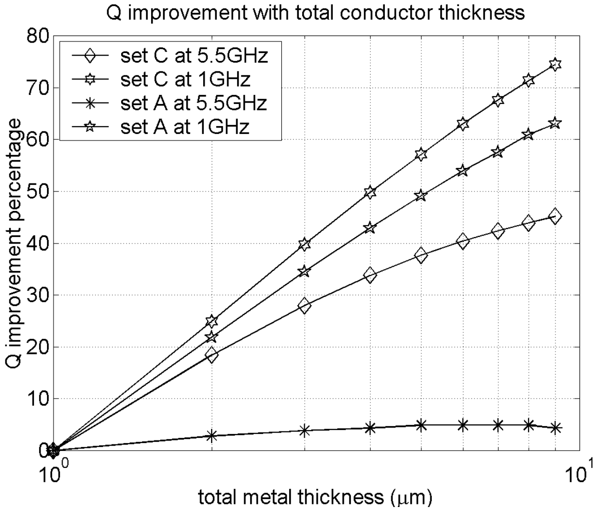


Figure. 6-17. **The percentage improvement in quality factor with increase in metal thickness at 1 GHz and 5.5 GHz for inductor L1, with and without post-process micromachining**

mechanical deformations change the inductance and hence affect the circuit performance. Residual stress differences in various films used in the interconnect fabrication causes the inductors to curl out of plane, such that the highest point of the inductor is above the plane of the chip. This out of plane curl is a function of the dimensions of the inductor and temperature. The variation of inductor performance with temperature has been studied by researchers [114] for conventional on chip inductors. Additional mechanical affects occur in suspended inductors that should be taken into account. Finite element simulations were carried out to verify the mechanical stability of the suspended inductors and predict curling due to residual stress and temperature. To the first order, two square (400 μm × 400 μm) five-turn inductors, one with single-sided and one with double-sided suspension, were analyzed. Thermomechanical simulations [115] were followed by FASTHENRY [111] simulations to compute the inductance after deformation. External shock to the inductor was simulated by subjecting the inductor structure to a static 9810 m/s^2 (100 G) of acceleration and calculating the inductance change. Motion due to external shock is very small (~ 0.5 μm) due to the extremely small mass of the inductor, on the order of 1 μg. Simulation was also performed on natural mechanical frequencies, which potentially can amplify the displacement from a shock, and can modulate the center frequency of a VCO. The first three mechanical vibration modes of the device are low frequency (8 to 23 kHz), and the effect of these modes can be compensated in the design of the PLL by a large loop gain. The higher frequency mechanical modes are difficult to excite in a packaged inductor due to the mechanical damping of the package. These resonances can be moved to higher frequencies by increasing the number of anchors. Table 6-4 summarizes the results of the mechanical simulation. The suspended inductors have a low mechanical dependence on inductance with temperature change because the relative displacement between adjacent turns is very small compared to the dimensions of the structure. The relative displacement between the turns is smaller in a single-suspended cantilever inductor, compared to the double-suspended inductor, even though the former has larger overall curl. This results in a lower inductance reduction for the single-suspended inductor after release.

Table 6-4: Summary of mechanical effects in 400 mm ´ 400 mm five-turn suspended inductors

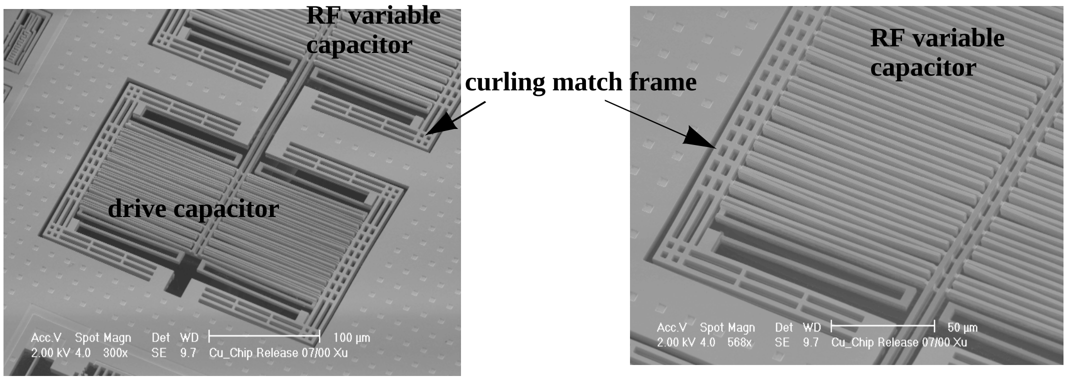
Simulation result	Single anchored inductor	Double anchored inductor
Nominal Inductance (nH)	4.824	4.918
Maximum out of plane curl (μm)	25.10	15.94
% Inductance change due to curl	-0.0070	-0.1036
1st Mechanical mode (kHz)	8.71	9.31
2nd Mechanical mode (kHz)	16.27	21.71
3rd Mechanical mode (kHz)	22.07	22.22
Temperature coefficient of inductance (ppm/^{o}C)	0.757	11.139
% Inductance change due to 100 G shock	-0.0162	-0.0173
Maximum deflection due to 100 G shock (μm)	0.5011	0.4543

Packaging MEMS on-chip inductors is still a challenge to the acceptance of MEMS RF inductors in industry, and innovations in economic packaging schemes are desirable.

6. 3 MEMS CAPACITORS

6. 3. 1 Parallel-Plate Tuning Capacitor Design

A variable tuning capacitor was also demonstrated with post-CMOS micromachining. The device consists of two sets of parallel-plate capacitors, as shown in Figure 6-18. One set is used for electrostatic force generation to move the mechanical structure, and the other set is used as the variable capacitor. There are two advantages to this type of capacitor. First, a MEMS capacitor can achieve a larger tuning range than generally used diode varactor, which around 100 fF. Second, the MEMS capacitor provides greater design freedom of the RF circuit topology. Both ports of the micromachined capacitor are floating and can be connected to any node in the circuit, unlike the diode where one node must always be connected to the substrate.


RF variable capacitor
curling match frame
drive capacitor
Acc.V Spot Magn Det WD 100 µm
2.00 kV 4.0 300x SE 9.7 Cu_Chip Release 07/00 Xu
RF variable capacitor
Acc.V Spot Magn Det WD 50 µm
2.00 kV 4.0 568x SE 9.7 Cu_Chip Release 07/00 Xu

(a) (b)

Figure. 6-18. Tunable micromachined capacitor.
(a) Actuator comb fingers across which the tuning voltage is applied to move the structure.
(b) Close-up of the variable capacitor.

6. 3. 2 Device Measurements

About 0.5 μm of displacement is obtained when 8 V is applied across the drive fingers. A change of 0.5 μm in the 1.5 μm normal gap corresponds to a 45 % change in capacitance. The static RF performance of the capacitors is characterized by measuring the static capacitance across the sense fingers. The capacitance of the device was derived from 1-port S-parameter measurements. Measurements were made using GSG waveguide probes connected to a Agilent 8752 network analyzer from 50 MHz to 20 GHz. Probe calibration was done by a CS-5 calibration substrate and the probe pads were de-embedded by making measurements on dummy pad structures (open and short). The capacitance difference between the device with oxide removed and the device with both oxide and silicon removed is shown in Figure 6-19. A low frequency, the capacitance of the device with only oxide removed capacitor is much higher than that of the device with both oxide and silicon removed. This difference is due to the change in parasitic capacitance to the substrate, which is parallel with the MEMS capacitor. However, the losses in the silicon at higher frequency make the impedance behavior more reactive and therefore it drops off drastically with frequency. The device with oxide and silicon removed has a nominal capacitance of about 800 fF. The summary of the micromechanical capacitor performance is presented in Table 6-5. The Smith chart of the S_{11} characteristic of the released capacitor is shown in Figure 6-20.

Mechanical motion of the micromachined capacitor was analyzed by applying 3 VAC and 3 VDC to the actuator fingers. The motion of the sense fingers was measured by the

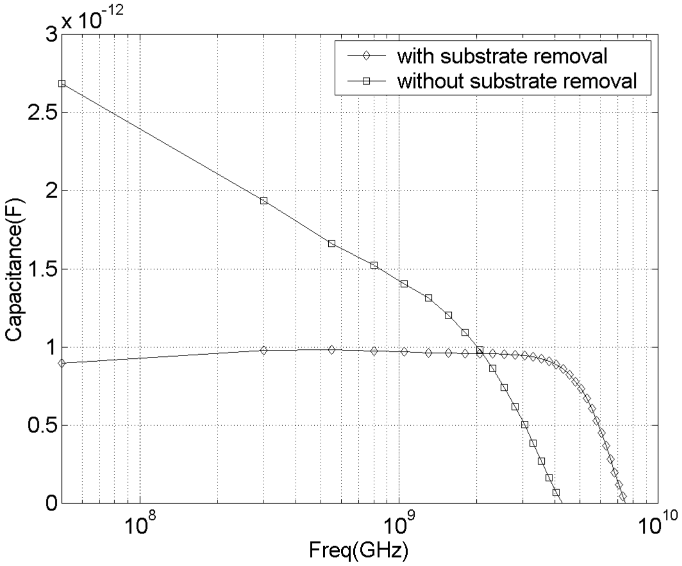


Figure. 6-19. **Comparison of the air gap capacitance of devices with oxide removed and with oxide and silicon removed.**

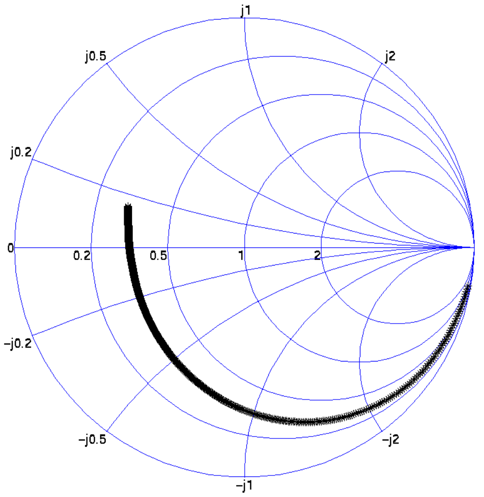


Figure. 6-20. **The S_{11} characteristic of the released micromechanical capacitor. On a Smith chart, larger semicircles indicate lower losses.**

MIT microvision system. The mechanical frequency response of the structure is shown in Figure 6-21. The mechanical resonant frequency of the system is 16.16 kHz.

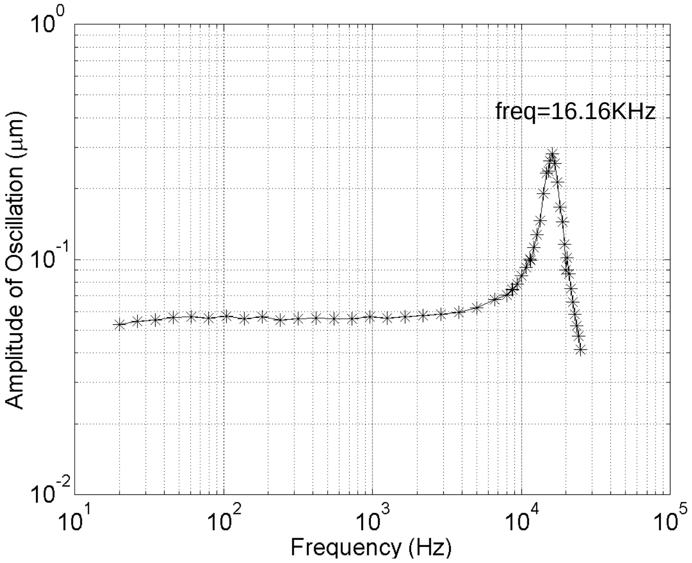


Figure. 6-21. Mechanical frequency response of the micromachined tunable capacitor. The second order system with the resonance frequency at16.16 kHz.

Table 6-5: Summary of the micromechanical capacitor characteristics.

Parameter	Design	Measured
Nominal Capacitance (fF)	370	800
Actuator displacement (μm)	0.5	0.5
Pull-in voltage (V)	-	8
Mechanical Resonant Frequency (KHz)	9.7	16.16
Q	-	7
Max Electrical frequency (GHz)	-	5

6. 3. 3 Discussion

The MEMS RF varactor demonstrates good capability as an on-chip component, but some limitations exist. First, due to the size of the capacitor, the long routing wires not only increase the series resistance connected to the capacitor, but also induce a large parasitic capacitance to the substrate and the top ground metal. The series resistance will reduce the Q of the inductor and the parasitic capacitance will reduce the tuning range. The capacitor is more lossy than what was reported for another MEMS capacitor fabricated by Yao [116]. Therefore, it is conclude that a very high aspect-ratio MEMS structure is required to reduce the MEMS varactor size.

Another conflicting requirement is the stiffness of the structure. To insure mechanical stability, the MEMS structure should be as stiff as possible in order to be immune to shock, acceleration and rotation induced capacitance change. On the other hand, to be driven by low voltage (< 5 V), the MEMS structure should be compliant. Therefore, in order to compensate for the capacitance changing due to the inertial movement, a feedback servo loop to drive the MEMS varactor is required.

6. 4 BULK MICROMACHINED ACCELEROMETER

Inertial sensing is one of the key applications of the MEMS industry [117], and it is an important research topic in post-CMOS micromachining [58][59][118]. Most commercial work is concentrated on thin-film structure sensors, such as the Analog Devices ADXL series [119], or on bulk silicon sensors which are not integrated into the CMOS processes. In this section, a novel technology [120] which integrates the bulk Si as an inertial sensor into post-CMOS micromachining is described, and results are reported.

6. 4. 1 Sensor Design

The layout of prototype sensors is show in Figure 6-22. The size of the proof mass is 1.6 mm × 1.3 mm. Other accelerometer designs have the circuitry surrounding the sensor, as in Figure 6-23. In the bulk-Si accelerometer design, the circuitry is located on the sensor itself, saving significant chip area. Currently, a pre-amplifier [118] is integrated with the proof mass. Therefore the chip size is minimized, and the chip layout is just large enough to hold the sensor, necessary interconnects and bonding pads. Moreover, the para-

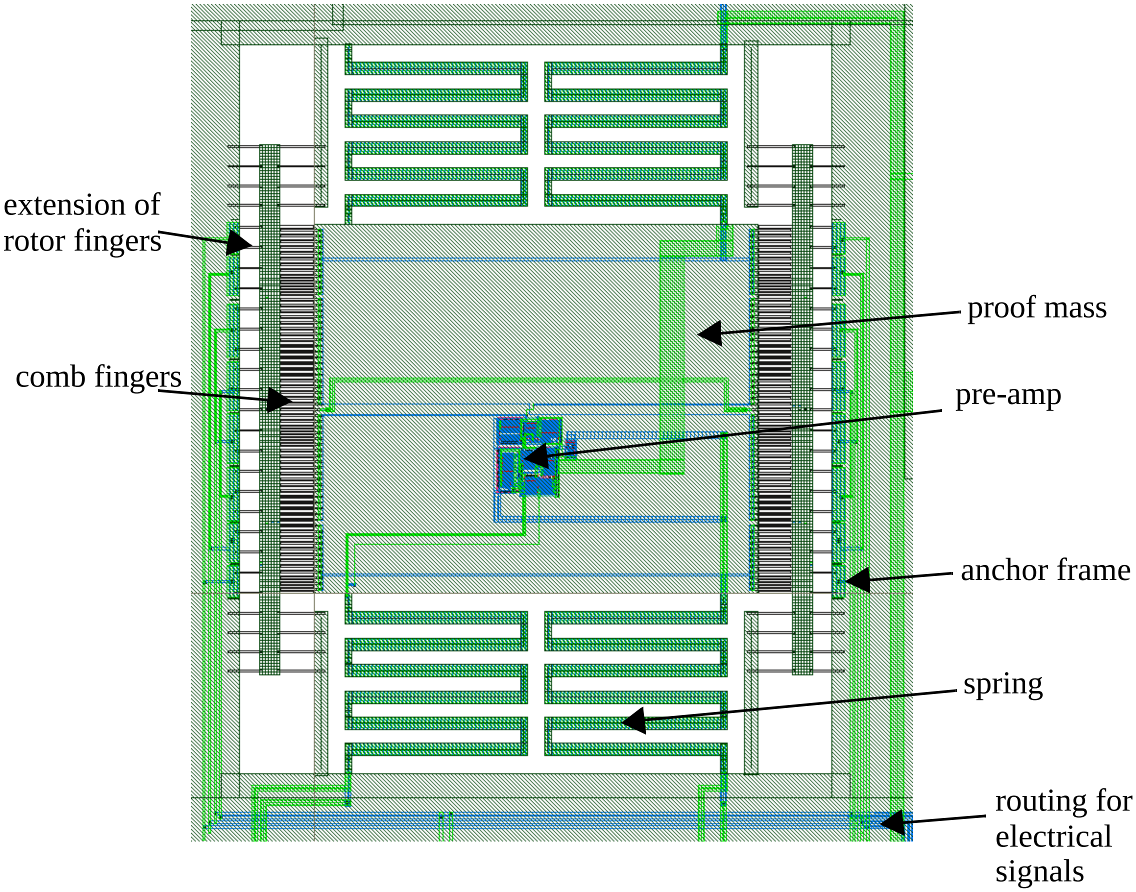

extension of rotor fingers
comb fingers
proof mass
pre-amp
anchor frame
spring
routing for electrical signals

Figure. 6-22. **Layout of the bulk-Si accelerometer.**

sitic capacitance associated with connections from sensors to the electronic circuitry can be minimized due to the shorter connections. Another benefit is that the interface electronics layout can be every symmetric since the sensing circuitry is located directly between the comb finger groups. Therefore, the input signals to the sensing circuit can be easily balanced.

6. 4. 2 Process flow

The complete process flow [120][121] is shown in Figure 6-24. A three-metal single-polysilicon CMOS process with CMP is used, as in Figure 6-24(a). Starting with CMOS dice fabricated in a foundry service, Figure 6-24(a), a Bosch DRIE anisotropic Si etch is

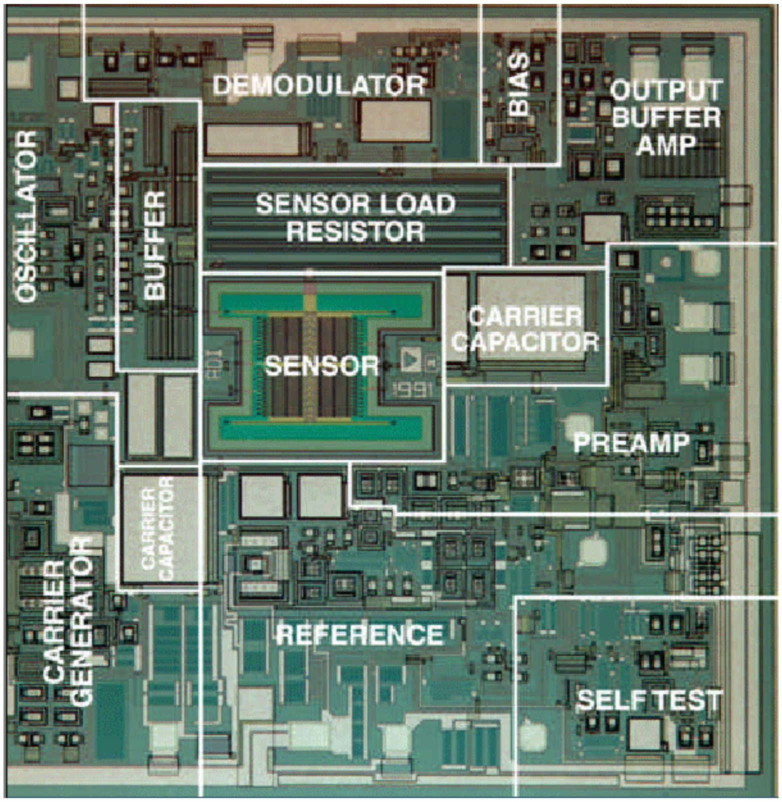

DEMODULATOR
BIAS
OUTPUT BUFFER AMP
OSCILLATOR
BUFFER
SENSOR LOAD RESISTOR
SENSOR
CARRIER CAPACITOR
PREAMP
CARRIER CAPACITOR
CARRIER GENERATOR
REFERENCE
SELF TEST

Figure. 6-23. **Chip photo of the Analog Devices ADXL-50 accelerometer, courtesy Dr. R. Payne, Analog Devices, Inc. .**

first performed from the back side of chips. The timed etch continues into the Si substrate stopping about 20 to 50 μm away from the interface of Si and dielectric, as in Figure 6-24(b). Then a CHF_3/O_2 anisotropic RIE of the dielectric layers from the front side results the structure as in Figure 6-24(c). Last a Si DRIE anisotropic etch is applied to the front side of chips this time. The mechanical structures are delineated by top CMOS interconnect metal layers. As described in Figure 6-24, instead of using an anisotropic Si etch to determine the separation of MEMS structures to the Si substrate plus an isotropic Si etch to release MEMS mechanical structures, the anisotropic etch of Si “releases” MEMS structures from peripheral anchors. The thicker structural Si yields better quality devices than thin-film alternatives in terms of the curvature and the size of proof mass under the

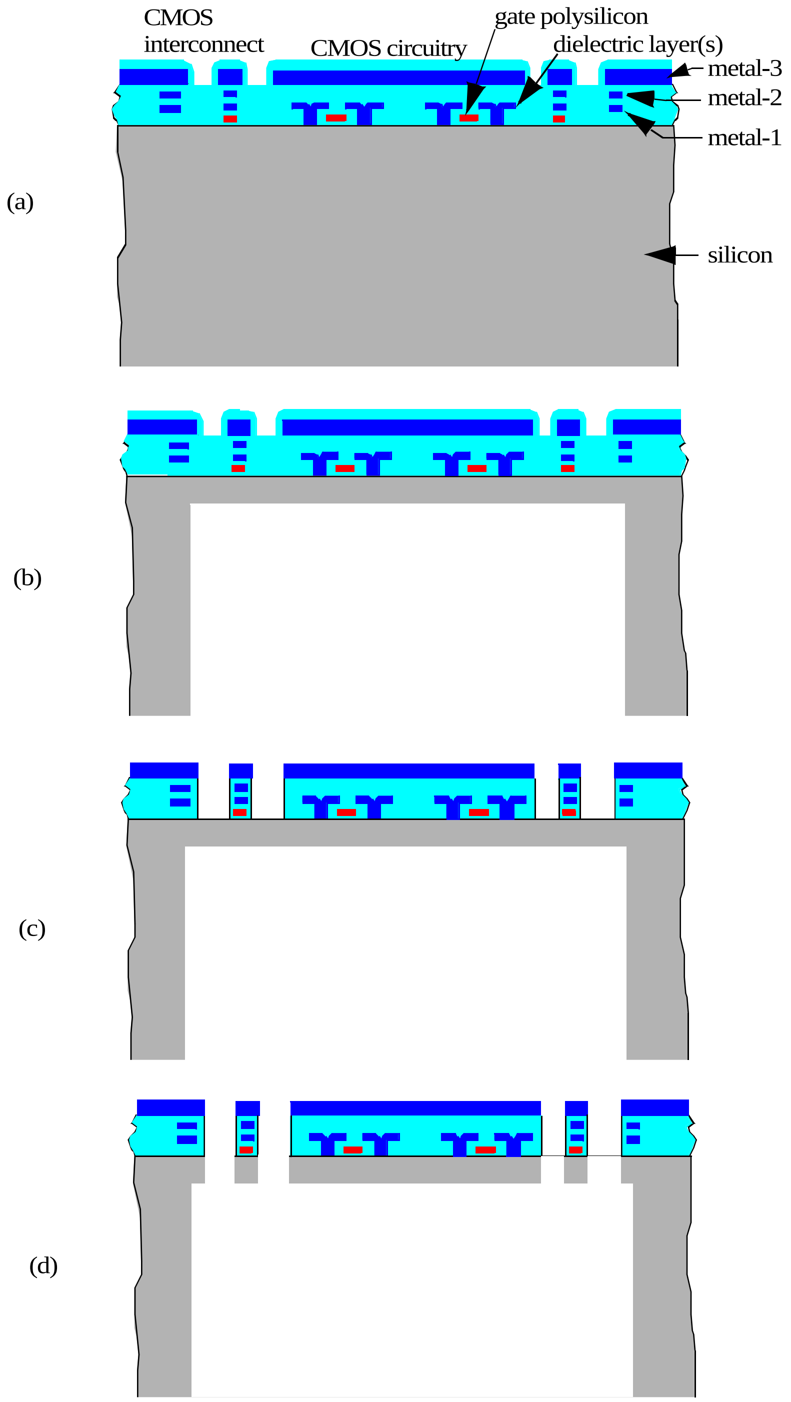
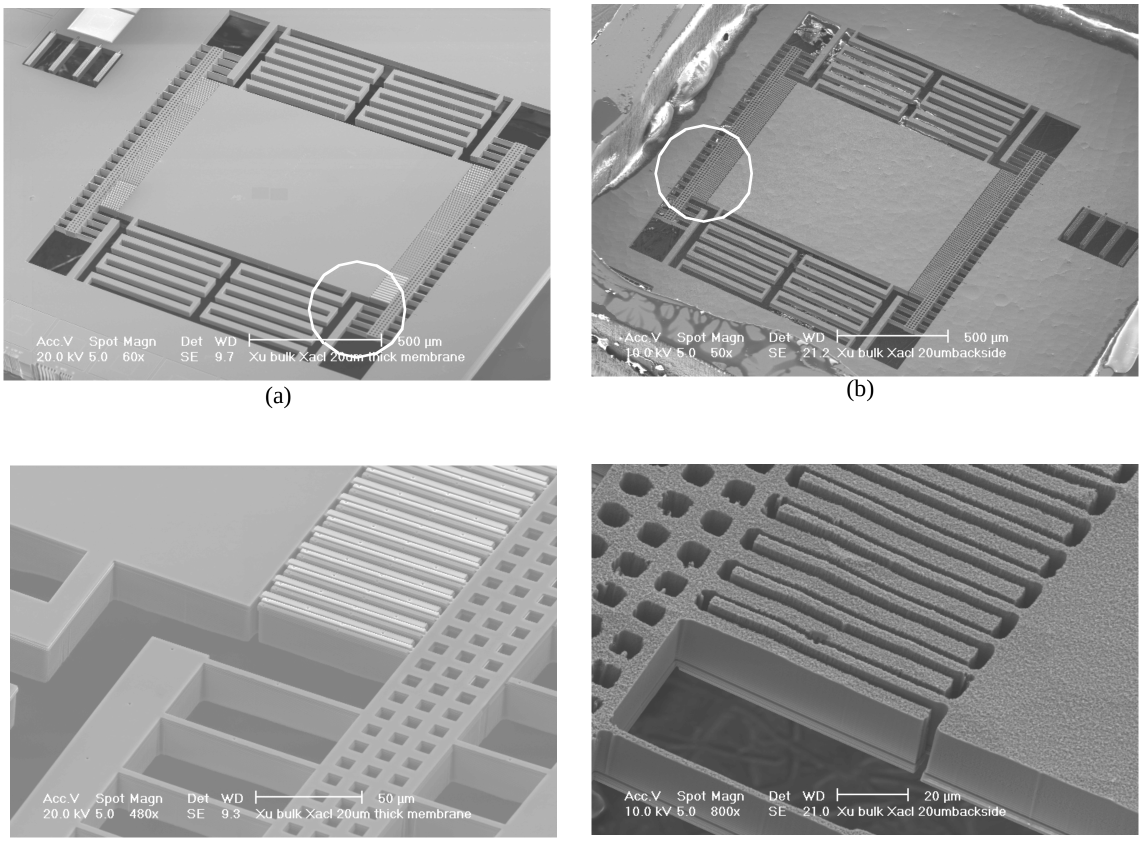

CMOS
interconnect
CMOS circuitry
gate polysilicon
dielectric layer(s)
metal-3
metal-2
metal-1
(a)
silicon
(b)
(c)
(d)

Figure. 6-24. Process flow of bulk-Si accelerometer.
(a) CMOS chips fabricated in foundry services.
(b) Backside DRIE Si anisotropic etch until only 20 to 50 mm of Si substrate left.
(c) Frontside dielectric etch to open the window for the Si etch.
(d) Frontside DRIE Si anisotropic etch.


Acc.V Spot Magn Det WD 500 µm
20.0 kV 5.0 60x SE 9.7 Xu bulk Xacl 20um thick membrane
Acc.V Spot Magn Det WD 500 µm
10.0 kV 5.0 50x SE 21.2 Xu bulk Xacl 20umbackside
Acc.V Spot Magn Det WD 50 µm
20.0 kV 5.0 480x SE 9.3 Xu bulk Xacl 20um thick membrane
Acc.V Spot Magn Det WD 20 µm
10.0 kV 5.0 800x SE 21.0 Xu bulk Xacl 20umbackside

(a) (b)

(c) (d)

Figure. 6-25. **Fabricated bulk CMOS accelerometer with a 25 mm thick Si proof mass.**
(a) Top view of front side.
(b) Bottom view of back side.
(c) Top view of enlarged part of (a) in white circle.
(d) Bottom view of enlarged part of (a) in white circle.

same physical layout area. However, the height-aspect-ratio of the etching process limits the thickness of the remaining Si with respect to mechanical gaps of comb fingers. With conservative design, a 20 : 1 aspect-ratio is possible.

6. 4. 3 Fabricated Device and Test Results

SEM photos of fabricated bulk-Si accelerometer devices are shown in Figure 6-25. The device is fabricated in the Agilent 0.5 μm CMOS process. The device structure is a 5 μm thick CMOS interconnect stack with 25 μm thick Si substrate underneath. The fin-

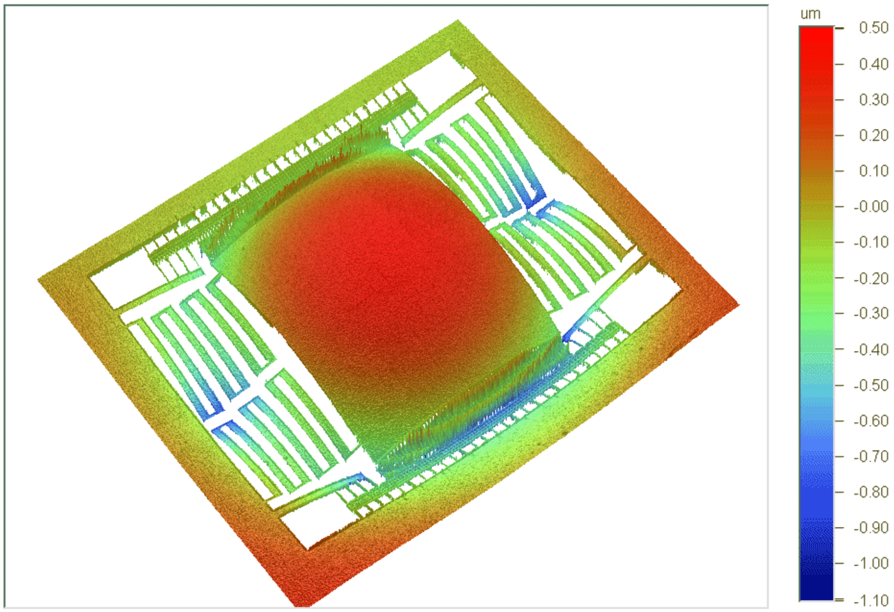


Figure. 6-26. **White-light interferometer measurement of the curvature of the bulk-Si accelerometer. The maximum out-of-plane curling is 0.5 mm upward on the proof mass, and 1.10 mm downward on the springs.**

ger gap is 1.8 µm. The stator and rotor fingers are 75 µm long but the stator fingers need another 90 µm extension to anchor to the chip frame. The white-light interferometeric measurement of the device is shown in Figure 6-26. The radius of curvature of the device is only 0.29 m for a 1.0 mm × 0.9 mm sensor proof mass.

The self-test mechanical frequency response is measured by a MIT Microvision system as in Figure 6-28. The self-test actuation is designed to produce force in the X-direction. However, the response in the Z-direction is due to the 400 nm Z-direction mismatch of fingers in the self-test structure. The Y-direction response is below instrument resolution and is not detected. The linearity and frequency response measurements of the seasoner output is measured with a Agilent 4395A spectrum analyzer with X-axis excitation on a Brüel & Kjær 4808 vibration exciter are shown in Figure 6-27 and Figure 6-29

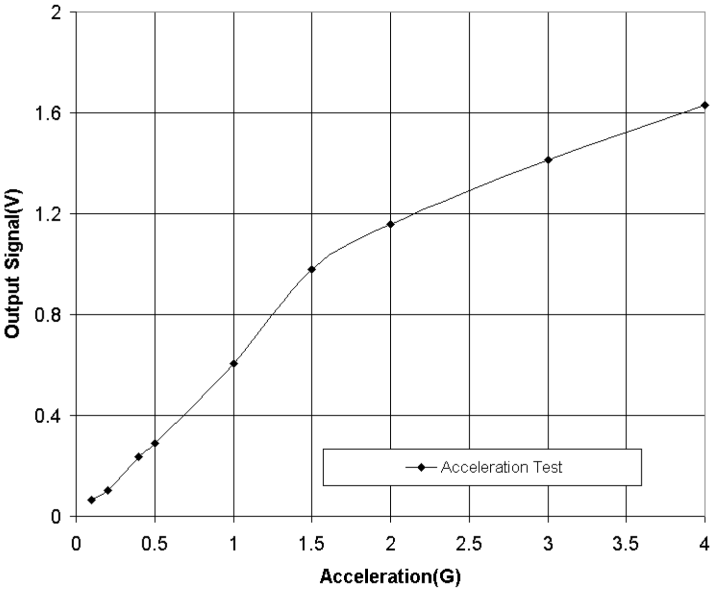


Figure. 6-27. The dynamic linearity of the CMOS bulk-Si accelerometer at 200 Hz.

respectively. The non-linear response in Figure 6-27 is due to the saturation at the output stage of the circuit. The resolution of the current design is $2\,mg/\sqrt{Hz}$ and the dynamic range is up to 4 g. The cross-axis sensitivity is -34 dB for in-plane disturbances, and -11 dB for out-of-plane disturbances. The measurement on the vibration exciter shows much lower 1st mode X-axis resonant frequency compared with the self-test measurement (with 18 V DC and 1 V AC driving voltage), 7 kHz, and the FEM simulation, 8.7 kHz. This is due to the package, PCB board, wires and fixtures on the exciter which have a much lower resonant frequency than the accelerometer. At the DRIE aspect ratio of 25:1.8, there is no need to adjust the general DRIE processing recipes, obtained by using photoresist as an etch mask.

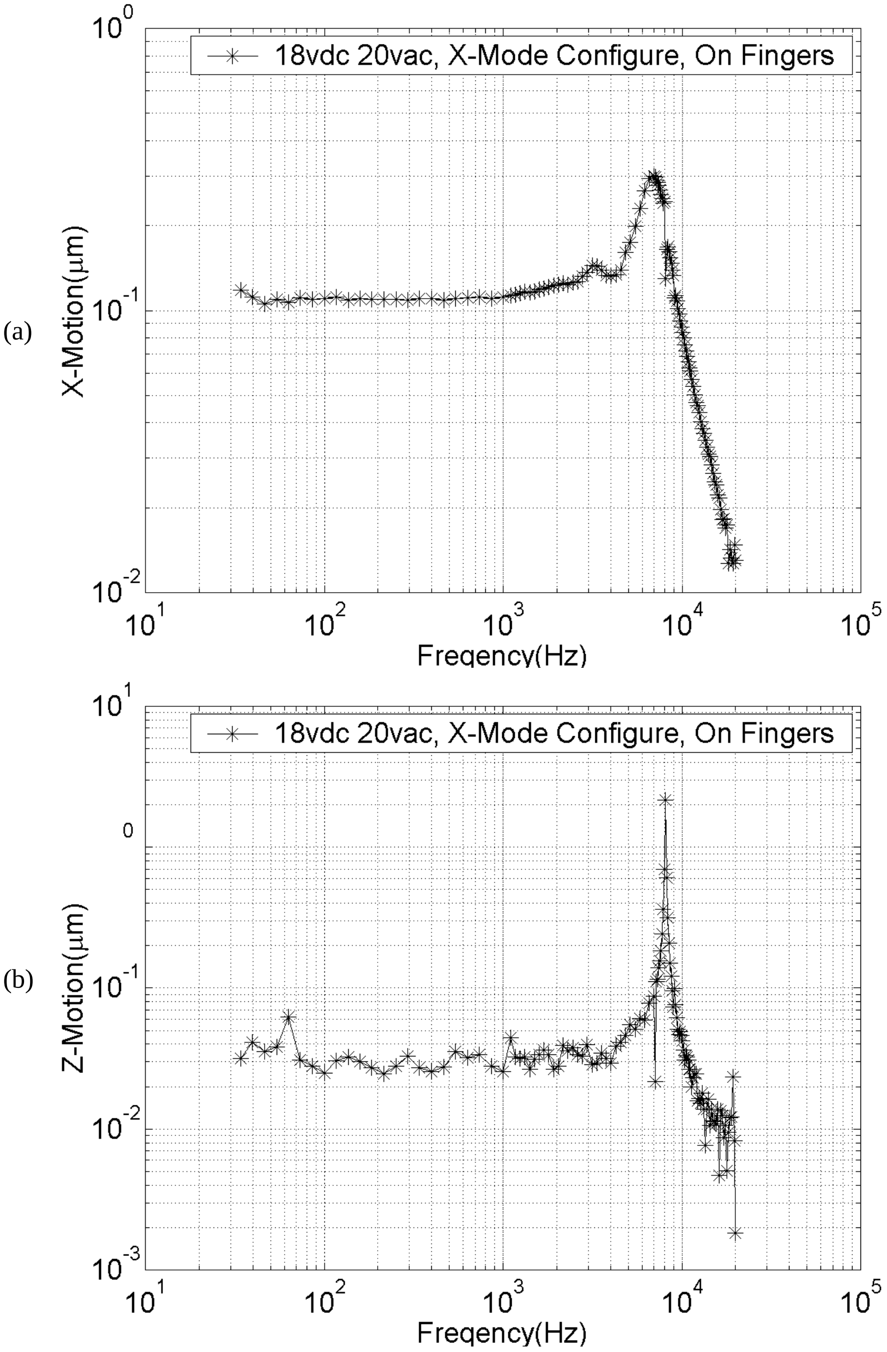


Figure. 6-28. **Mechanical response of the bulk Si-CMOS accelerometer with self-test excitation. The testing condition is 18 VDC with 1 VAC.**
(a) resonant at X direction, with resonant frequency around 7 kHz.
(b) resonant at Z direction, with resonant frequency around 8 kHz.

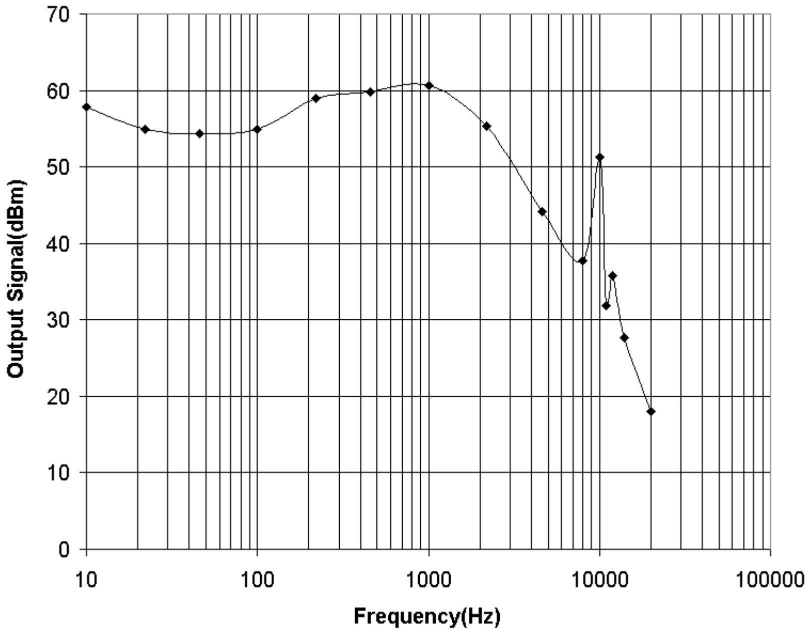


Figure. 6-29. **The frequency response of the bulk-Si CMOS accelerometer.**

7

Conclusions

In this thesis, we have demonstrated a completed post-CMOS microfabrication flow that includes both surface and bulk micromachining. This process flow has been characterized by the Box-Behnken method, a widely used design of experiment method. Experimental mathematical models to represent the effect of each processing parameter have been established. This models can precisely predict the etching result when processing parameters vary within the tested space, and “brute force” to optimize the processing is not required. This process flow has been successfully demonstrated in various CMOS foundry processes, including:

- Agilent 0.5 μm three-metal (Al) SiO_2 dielectric process,
- Agilent 0.35 μm four-metal layer SiO_2 dielectric process,
- Taiwan Semiconductor Manufacturing Company (TSMC) 0.35 μm three-metal (Al) SiO_2 dielectric process,
- Austria Microsystems (AMS) 0.5 μm three-metal (Al) SiO_2 dielectric process,
- United Microelectronics Corp. (UMC) 0.18 μm 6-metal (Cu) low-K dielectric

process,

- IBM 0.5 μm three-metal (Al) SiO_2 dielectric process.

A crab-leg resonator demonstrates the micromachining in each CMOS foundry process. The results are listed in Figure 7-1.

To design thin-film MEMS structures with post-CMOS micromachining, a set of design rules is generated at the end of Chapter 3. The fundamental layout elements of MEMS structures are included in the design rules. These are gap undercut rules, hole undercut rules and large opening undercut rules. Release of all CMOS-MEMS designs can be decomposed into these three structures. These rules can be represented into CAD systems, such as Cadence's DIVA or Dracula format. Therefore, concurrent integrated MEMS structure designs and electronic system designs can be accomplished.

The major issues for post-CMOS micromachining are cleaning of polymer generation during the process, adjusting the processing parameter settings for different CMOS foundries, and avoiding micromasking in wafer-scale processing. Process parameters are set under the guidelines of models developed in previous chapters.

7. 1 TYPICAL APPLICATIONS

Two applications, a bulk micromachined accelerometer and on-chip RF passive components, are shown in the Chapter 6. Other devices fabricated in this process includes the following: thin-film inertial sensors, which include accelerometers (Figure 7-2(a)(b), Figure 7-3(a)(b)(c)), gyro (Figure 7-2(c)) and inertial measurement system (Figure 6-7),

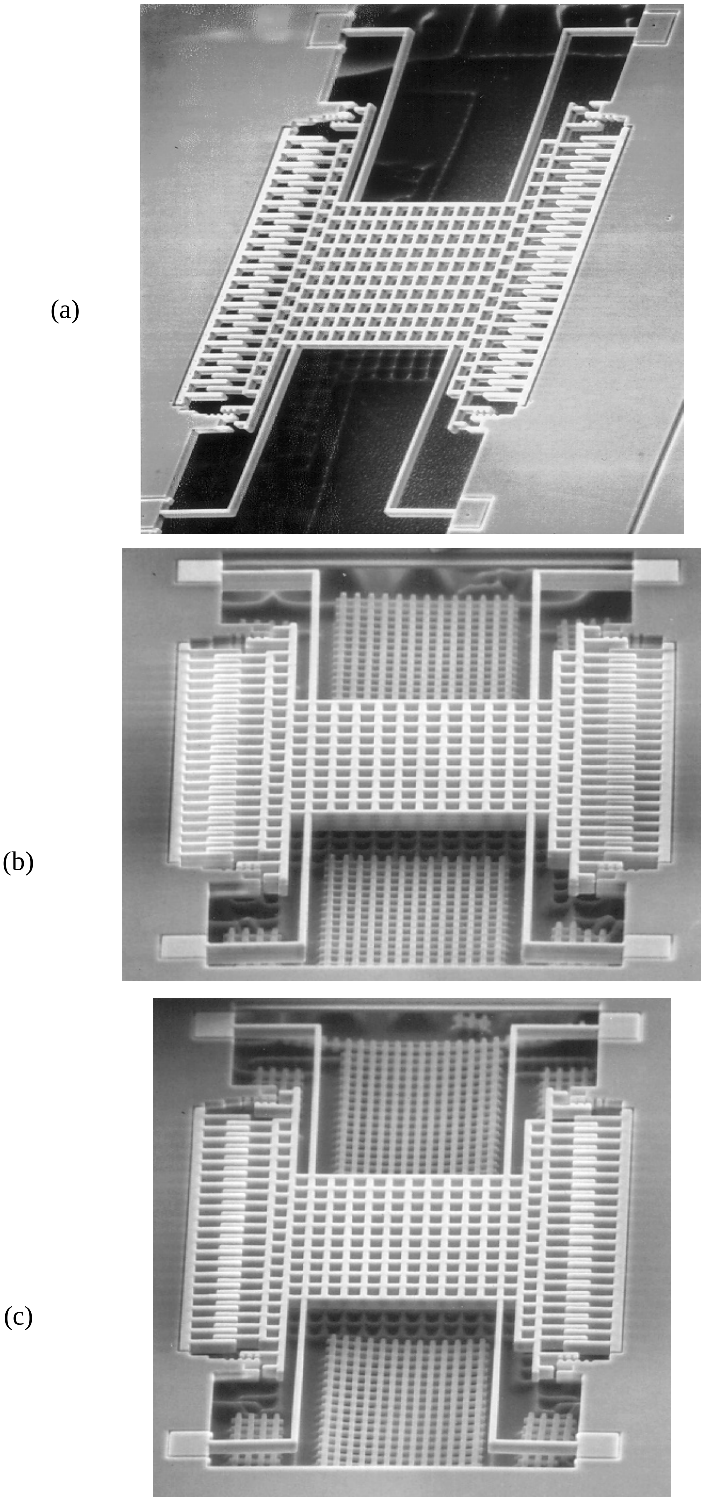


Figure. 7-1. Successfully fabricated crab-leg resonator with different CMOS foundry processes.
(a) Agilent 0.6 μm Al interconnect SiO_2 dielectric CMOS process.
(b) Agilent 0.35 μm Al interconnect SiO_2 dielectric CMOS process.
(c) TSMC 0.35 μm Al interconnect SiO_2 dielectric CMOS process.

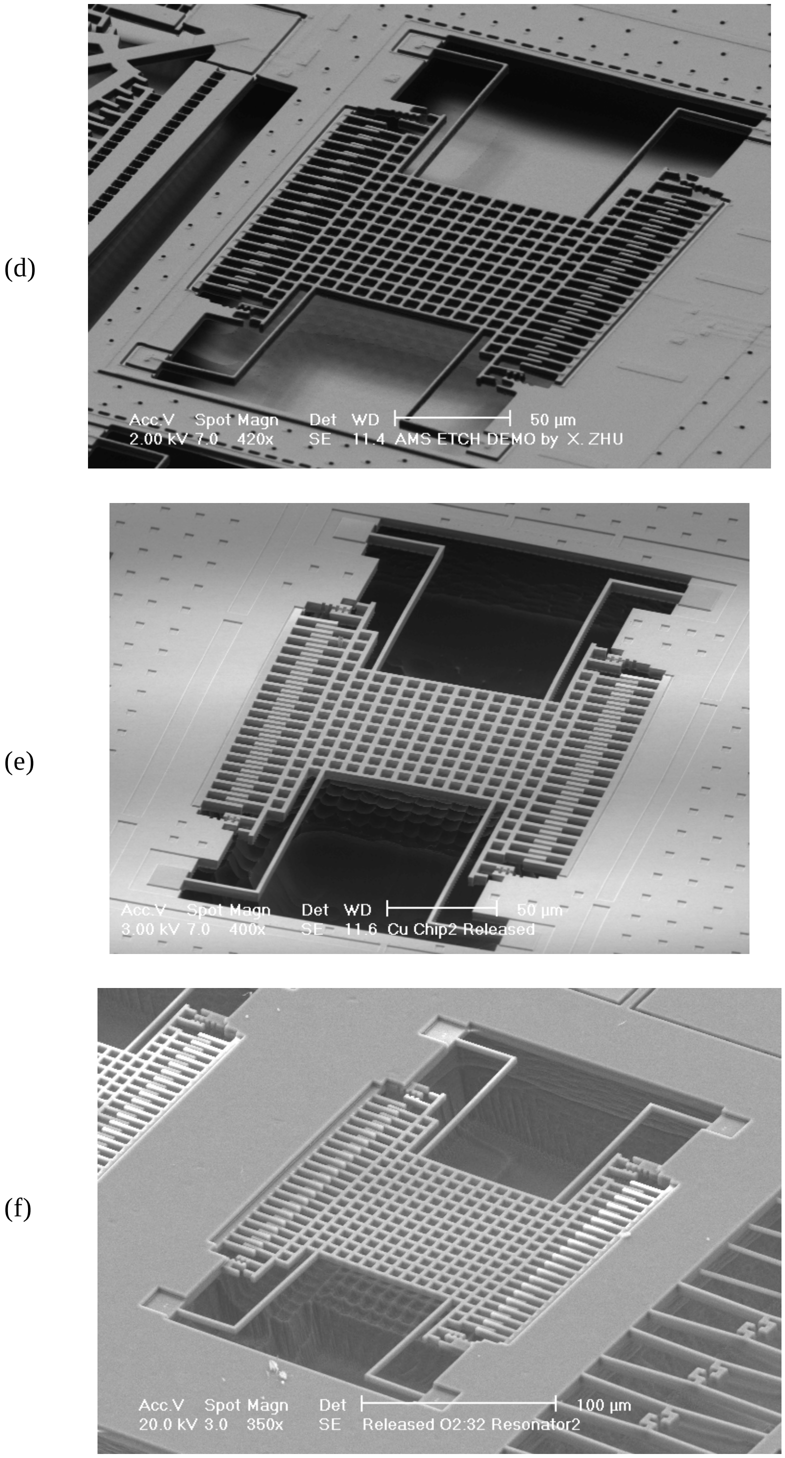

(d)
Acc.V Spot Magn Det WD 50 µm
2.00 kV 7.0 420x SE 11.4 AMS ETCH DEMO by X. ZHU
(e)
Acc.V Spot Magn Det WD 50 µm
3.00 kV 7.0 400x SE 11.6 Cu Chip2 Released
(f)
Acc.V Spot Magn Det 100 µm
20.0 kV 3.0 350x SE Released O2:32 Resonator2

Figure. 7-1 Continued. **Successfully fabricated crab-leg resonator with different CMOS foundry processes.**
(d) AMS 0.5 μm Al interconnect SiO_2 dielectric CMOS process.
(e) UMC 0.18 μm Cu interconnect low-K dielectric CMOS process.
(f)IBM SiGe 0.5 μm Al interconnect SiO_2 dielectric CMOS process, courtesy K. Frederick.

infrared sensor [122], data storage devices [123], stress sensor [79], material property test structures [89], RF on-chip components [101], actuators [31], acoustic device - membrane structure [124], and MEMS Filter [125].

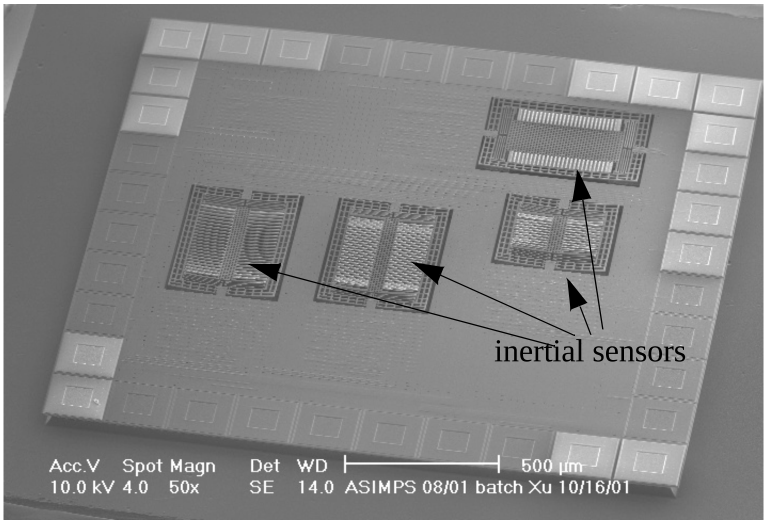

inertial sensors
Acc.V Spot Magn Det WD 500 µm
10.0 kV 4.0 50x SE 14.0 ASIMPS 08/01 batch Xu 10/16/01

Figure. 7-4. **Integrated inertial measurement system.**

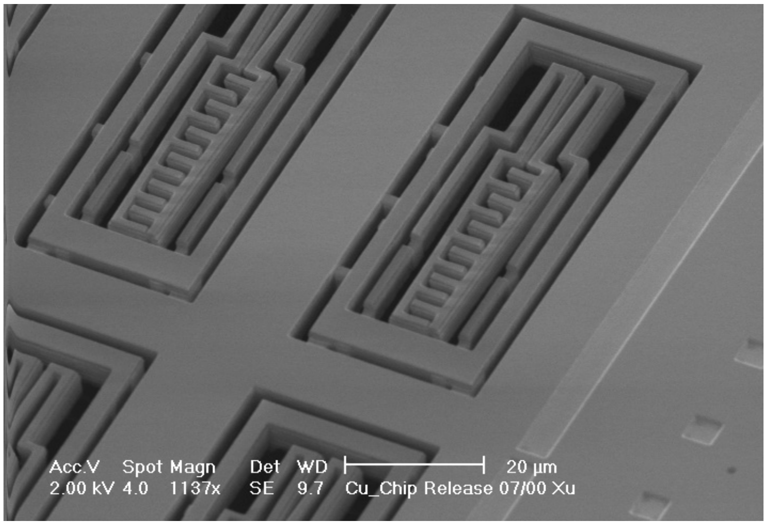

Acc.V Spot Magn Det WD 20 µm
2.00 kV 4.0 1137x SE 9.7 Cu_Chip Release 07/00 Xu

Figure. 7-5. **Infrared sensor by capacitive sensing of lateral curl with the change of the structure's temperature.**

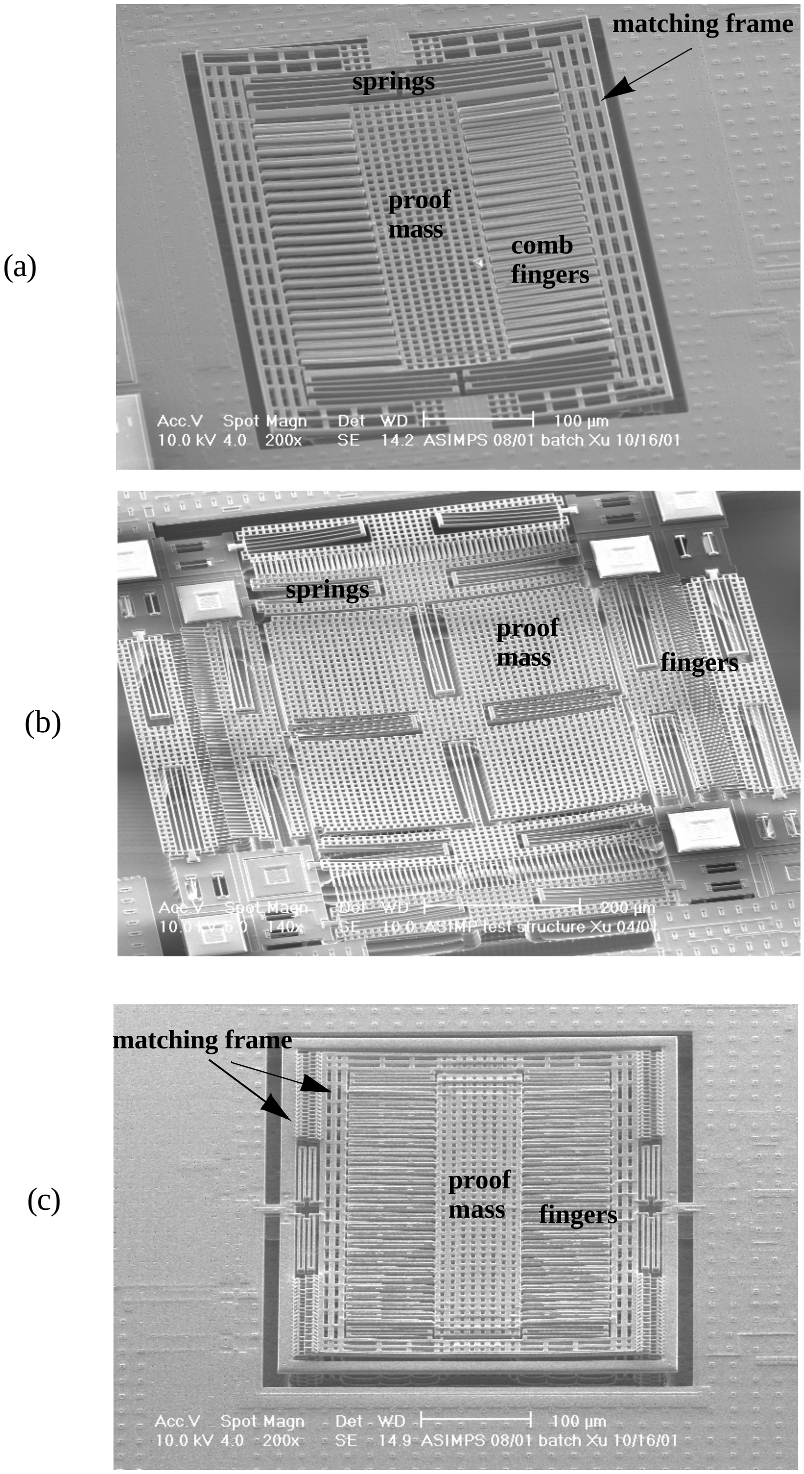

(a)
matching frame
springs
proof mass
comb fingers
Acc.V Spot Magn Det WD 100 µm
10.0 kV 4.0 200x SE 14.2 ASIMPS 08/01 batch Xu 10/16/01
(b)
springs
proof mass
fingers
Acc.V Spot Magn Det WD 200 µm
10.0 kV 6.0 140x SE 10.0 ASIMP test structure Xu 04/01
(c)
matching frame
proof mass
fingers
Acc.V Spot Magn Det WD 100 µm
10.0 kV 4.0 200x SE 14.9 ASIMPS 08/01 batch Xu 10/16/01

Figure. 7-2. **Thin-film type inertial sensors.**
(a) Lateral accelerometer with one dimension.
(b) Lateral accelerometer with integrated two dimensions, permission from M. Kranz of Morgan Research.
(c) Vertical-axis gyroscope.

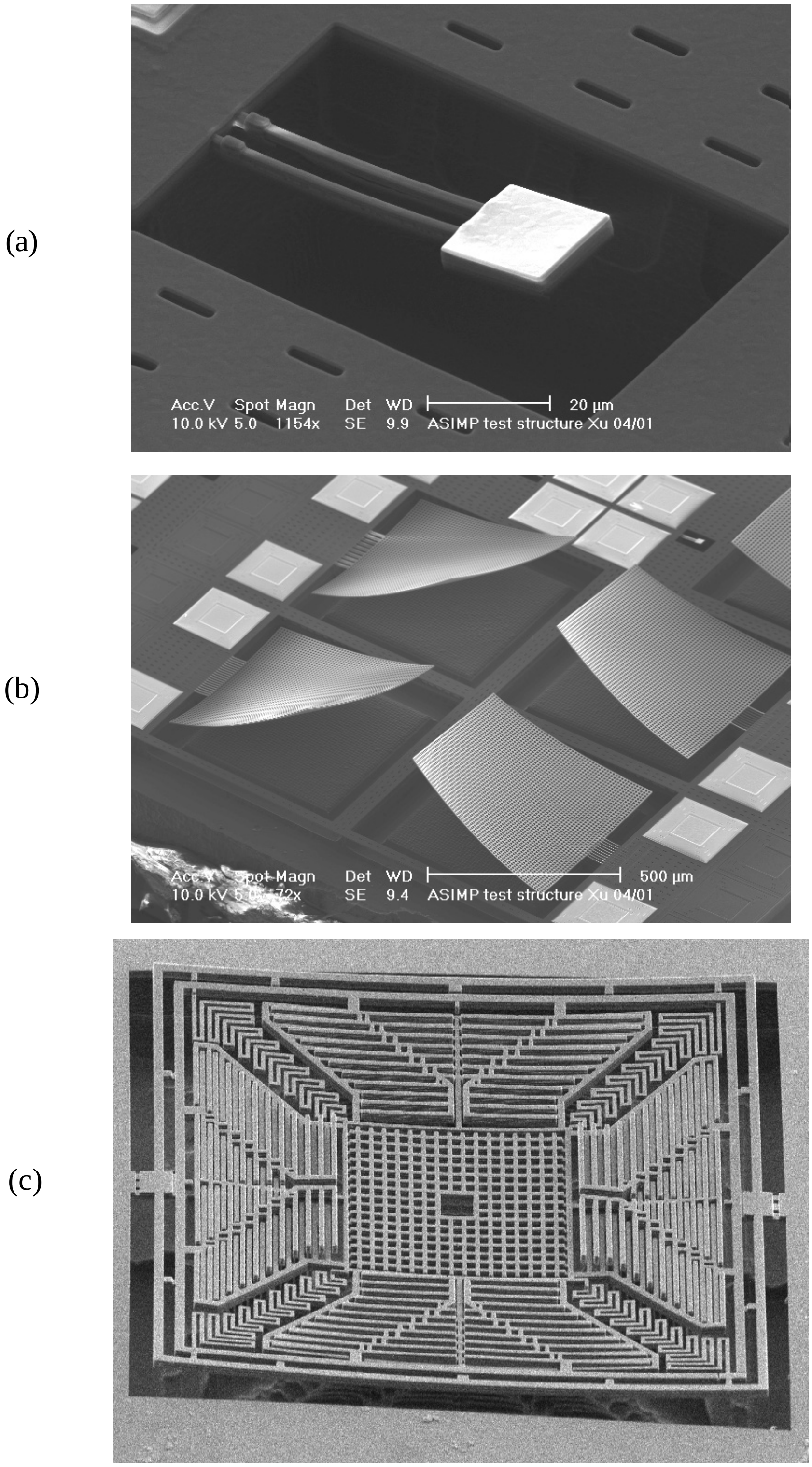

(a)
Acc.V Spot Magn Det WD 20 µm
10.0 kV 5.0 1154x SE 9.9 ASIMP test structure Xu 04/01
(b)
Acc.V Spot Magn Det WD 500 µm
10.0 kV 5.0 72x SE 9.4 ASIMP test structure Xu 04/01
(c)

Figure. 7-3. **Vertical-axis accelerometers.**
(a) By polysilicon-piezoresist sensor, permission from B. Warneke of BSAC.
(b) By polysilicon-piezoresist sensor, permission from B. Warneke of BSAC.
(c) By capacitive sensing.

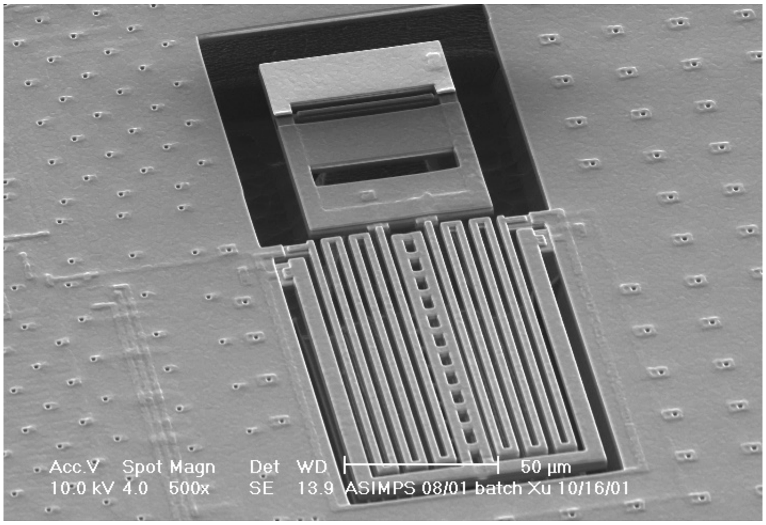

Acc.V Spot Magn Det WD 50 µm
10.0 kV 4.0 500x SE 13.9 ASIMPS 08/01 batch Xu 10/16/01

Figure. 7-6. **Parallel-plate actuator used as read/write head arm in the MEMS based data storage system.**

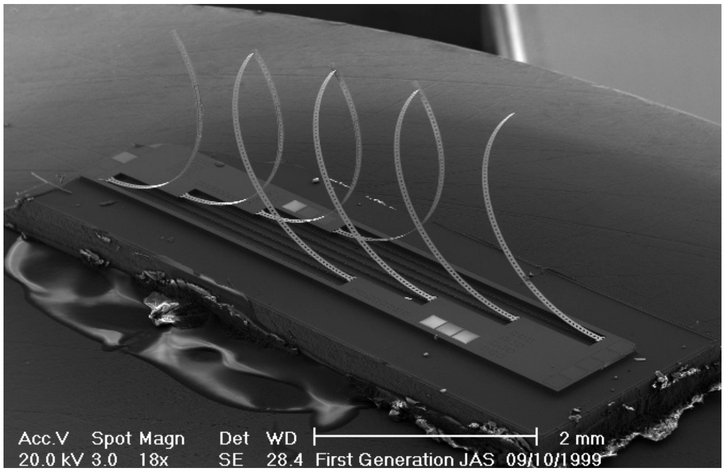

Acc.V Spot Magn Det WD 2 mm
20.0 kV 3.0 18x SE 28.4 First Generation JAS 09/10/1999

Figure. 7-7. **Cilia for study of a joint angle sensor.**

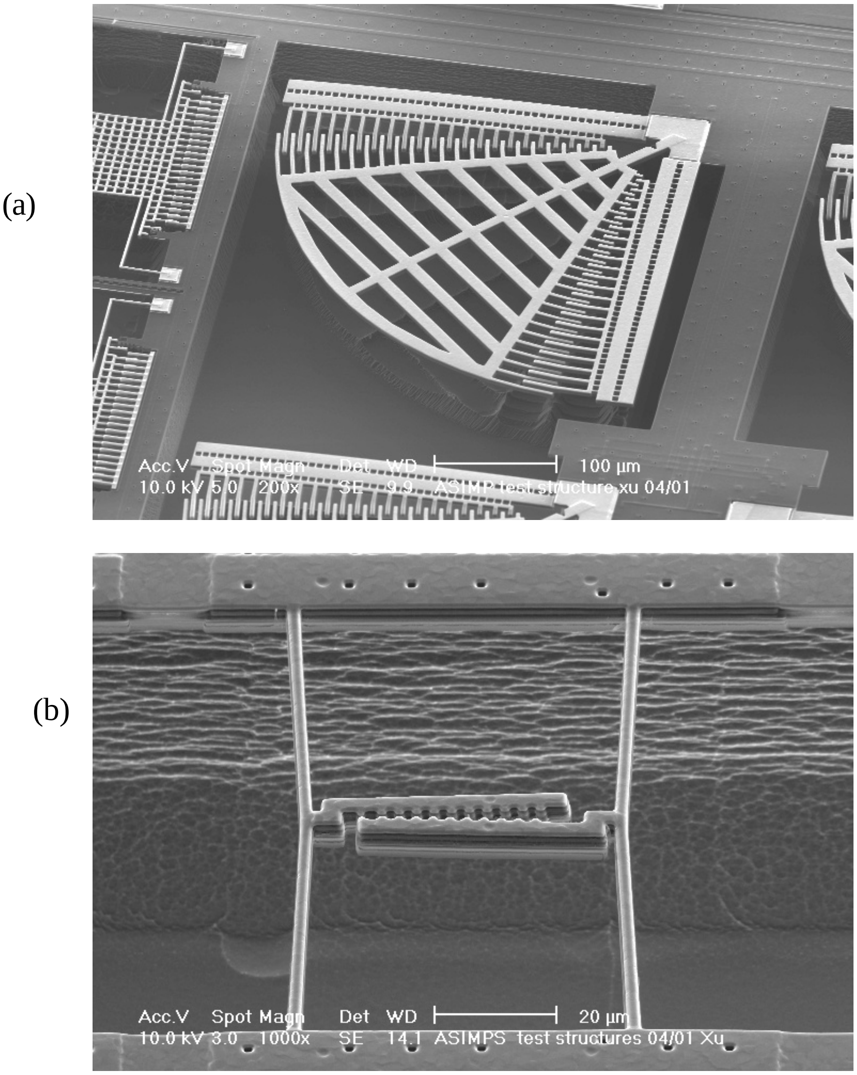

(a)
Acc.V Spot Magn Det WD 100 µm
10.0 kV 5.0 200x SE 9.9 ASIMP test structure xu 04/01
(b)
Acc.V Spot Magn Det WD 20 µm
10.0 kV 3.0 1000x SE 14.1 ASIMPS test structures 04/01 Xu

Figure. 7-8. **Material property testing structures.**
(a) Failure/reliability testing structure
(b) Residual stress testing structure.

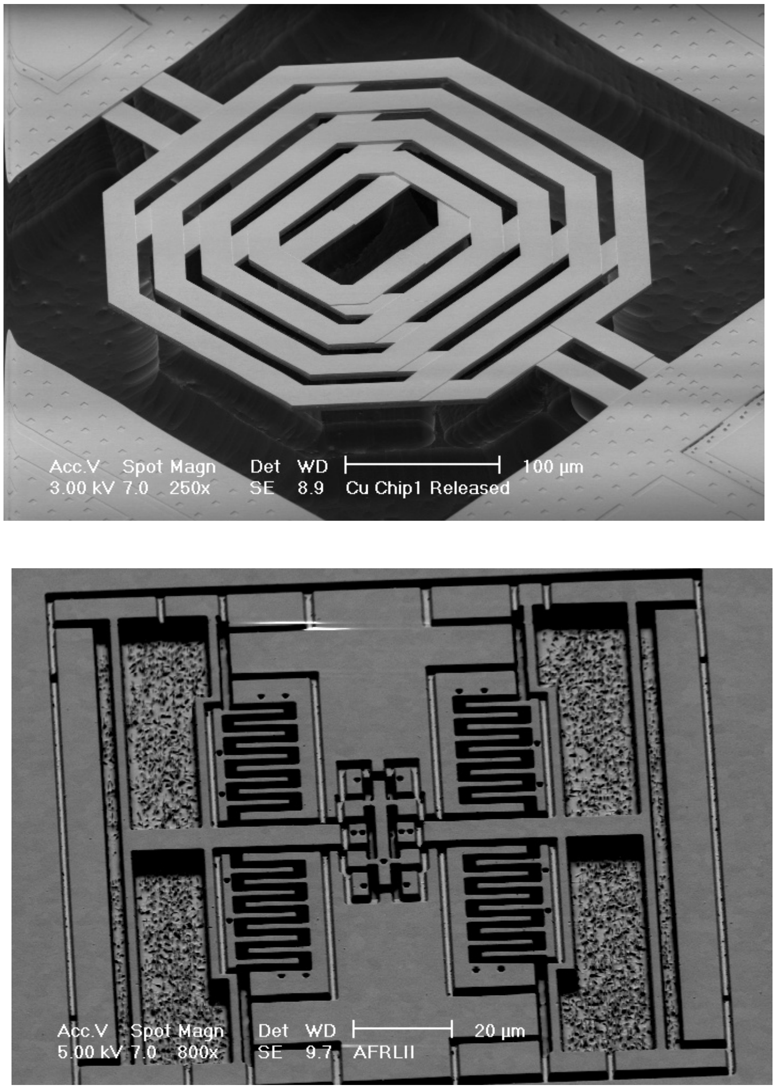

Acc.V Spot Magn Det WD 100 µm
3.00 kV 7.0 250x SE 8.9 Cu Chip1 Released
Acc.V Spot Magn Det WD 20 µm
5.00 kV 7.0 800x SE 9.7 AFRLII

Figure. 7-9. **On-chip RF components.**
(a) RF transformer.
(b) high frequency resonator, permission from T. Renz of AFRL.

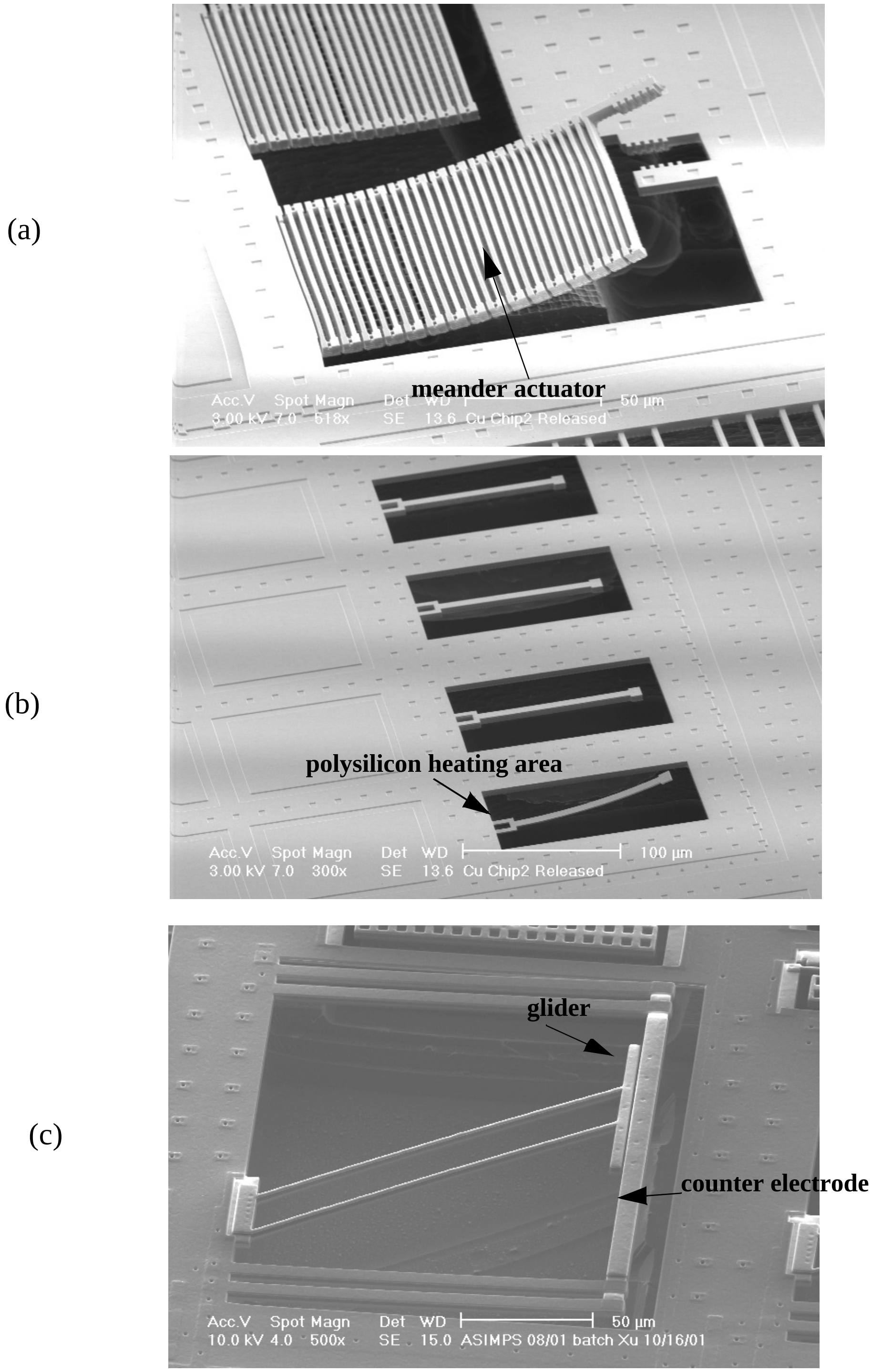

(a)
meander actuator
Acc.V Spot Magn Det WD 50 µm
3.00 kV 7.0 618x SE 13.6 Cu Chip2 Released
(b)
polysilicon heating area
Acc.V Spot Magn Det WD 100 µm
3.00 kV 7.0 300x SE 13.6 Cu Chip2 Released
(c)
glider
counter electrode
Acc.V Spot Magn Det WD 50 µm
10.0 kV 4.0 500x SE 15.0 ASIMPS 08/01 batch Xu 10/16/01

Figure. 7-10. **Actuators.**
(a) Electrostatic actuated meander structure.
(b) Thermal actuated tip for AFM.
(c) Electrostatic actuated glider.

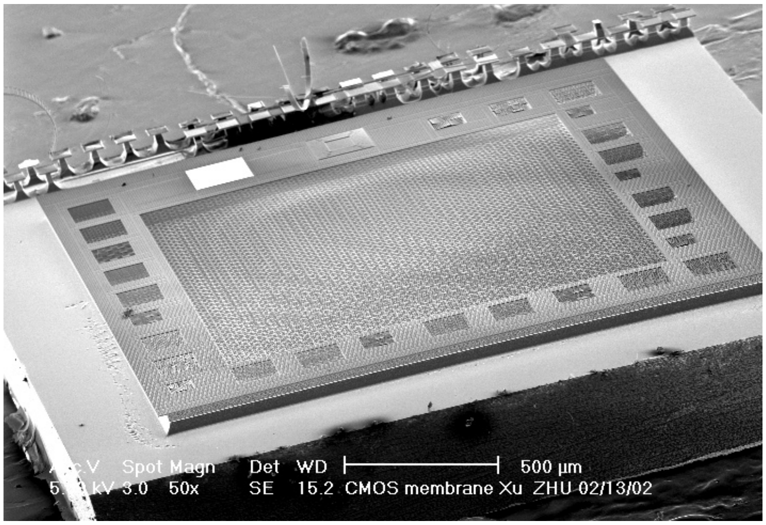

Acc.V Spot Magn Det WD 500 µm
5.0 kV 3.0 50x SE 15.2 CMOS membrane Xu ZHU 02/13/02

Figure. 7-11. Acoustic device made of CMOS metal interconnect membrane.

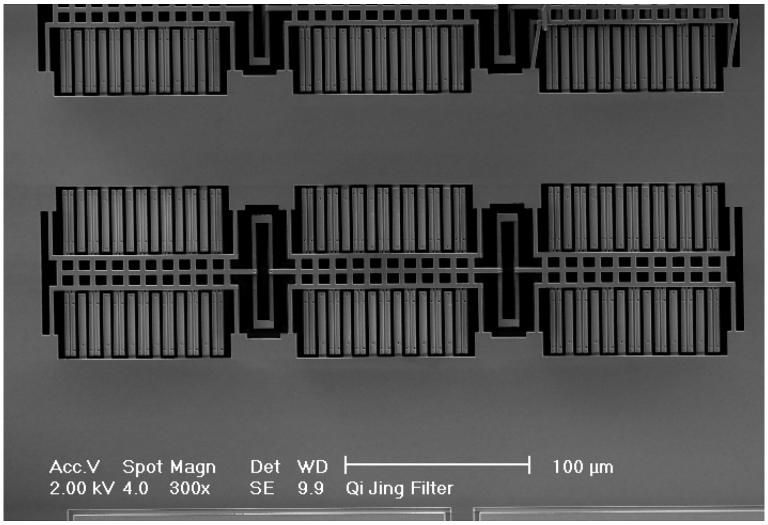

Acc.V Spot Magn Det WD 100 µm
2.00 kV 4.0 300x SE 9.9 Qi Jing Filter

Figure. 7-12. Bandpass circuit filter implemented by cascaded MEMS resonant structures.

7. 2 FUTURE WORK

This thesis provides an overview of post-CMOS micromachining, and it covers the issues in the processing development. A protocol (concluded as design rules) for the MEMS users has been established. Practical applications of this technique has been demonstrated.

For more efficient MEMS designs in the future, more accurate design rules are preferred. New test structure designs should be in the vicinity of the data generated by the results from Chapter 4, assuming use of the same processing parameters.

To establish a comprehensive material database, a complete scenario should be included in test structures, such as test structures with N-Well, N+, P+, and removal of field oxide by putting active layer in the design. The data on the variation of CMOS MEMS structures and post-CMOS process should also be collected. With such a complete database, the mechanical behavior of the device can be predicted before it is fabricated.

Advanced high performance circuit design for interfacing to post-CMOS micromachined devices is still a challenge. For example, with inductor values over 10 nH, the phase noise of a VCO over -100 dBc/Hz can be achieved theoretically; Another example is for the bulk-micromachined accelerometer, the theoretical noise floor is about $10\mu g/\sqrt{Hz}$. Much improvement for the current circuit noise is required.

In summary, post-CMOS micromachining is a promising technique to accelerate the commercialization of MEMS technology, and “There is plenty of room at the bottom!”[4].

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APPENDIX A:

DETAILS FOR POST-CMOS MICROMACHINING

1. Dielectric etch by Plasma-Therm 790 parallel-plate RIE system

Table A-1: Anisotropic SiO_2 Dielectric Etch Processing Parameters

Procesinng Parameters	Parameter Settings
CHF_3 (sccm)	22.5
O_2 (sccm)	16
Pressure(mTorr)	125
Time (min)	125
Power(W)	110
DC bias(V)	320~340

Table A-2: Anisotropic Novellus FSG Low-K Dielectric Etch Processing Parameters

Procesinng Parameters	Parameter Settings
CHF_3 (sccm)	22.5
O_2 (sccm)	32
Pressure(mTorr)	125
Time (min)	125
Power(W)	110
DC bias(V)	430~440

2. Deep Si trench etch by STS time-multiplexed DRIE system

Table A-3: Procesing Parameters for Anisotropic Silicon Etch Process

Parameters	Etch cycle settings	Passivation cycle settings
SF_6 flow (sccm)	130	-
O_2 flow (sccm)	20	-
C_4F_8 flow (sccm)	-	120
Cycle time (sec)	7	5
Platen power(W)	10	-
Coil power(W)	600	600
Pressure (mTorr)	15	15
APC angle (%)[a]	41	51
DC bias(V)	54	-
Number of cycles	125	

a. Pressure is set in the proccess and APC value is measured.

Etch rate: 1.5 μm/min

3. Isotropic Si etch by STS time-multiplexed DRIE system

Table A-4: Procesing Parameters for Anisotropic Silicon Etch Process

Parameters	Etch cycle settings
SF_6 flow (sccm)	130
O_2 flow (sccm)	30
Platen Power (W)	12
Coil Power (W)	600
Pressure (mTorr)	50
APC angle (%)[a]	84
DC bias (V)	60
Processing time (min)	5

a. Pressure is set in the proccess and APC value is measured.

4. Ar Cleaning after Si Isotropic Etch by STS time-multiplexed DRIE system[1]

Table A-5: Processing Parameters for Argon Clean

Parameter	Process Parameters
Argon (sccm)	50
Pressure (mTorr)[a]	7.6
Time (min)	20
Coil Power (W)	800
Platen Power (W)	25
APC angle (%)	75
DC Bias (V)	27

a. APC value is set, and pressure is measured.

5. O2 Cleaning after Si Isotropic Etch by STS time-multiplexed DRIE system[2]

Table A-6: Processing Parameters for Argon Clean

Parameter	Process Parameters
O_2 (sccm)	50
Pressure (mTorr)[a]	16
APC angle (%)	84
Time (min)	10
Coil power(W)	800
Platen power (W)	12
DC bias	30

a. APC value is set, and pressure is measured.

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[1] Strongly recommended step for Cu low-K CMOS, not required for Al SiO_2 CMOS

[2] Recommended step to cleaning polymers on the microstructures, especially the DRIE passivation polymers.